Custom SoC(ASIC)

Optimise the value of your products with Socionext's custom SoC development

Talk to us about your custom SoC development needs.

Socionext continues to expand its unique solutions for custom SoC development, reducing project risk and adding value to your products.

Through our ability to support an increasing range of IP and process technology options, Socionext can address the needs of a wider range of customers and applications than ever before.

services.

For customers considering their first SoC development, Socionext provides a range of support options. These include consulting services at all phases of the development, from initial concept definition to specification of the corresponding final SoC product. Our expertise in all aspects of the SoC design process, and our access to world-leading technologies enables us to partner with you in ensuring the optimal solutions to add value to your products.
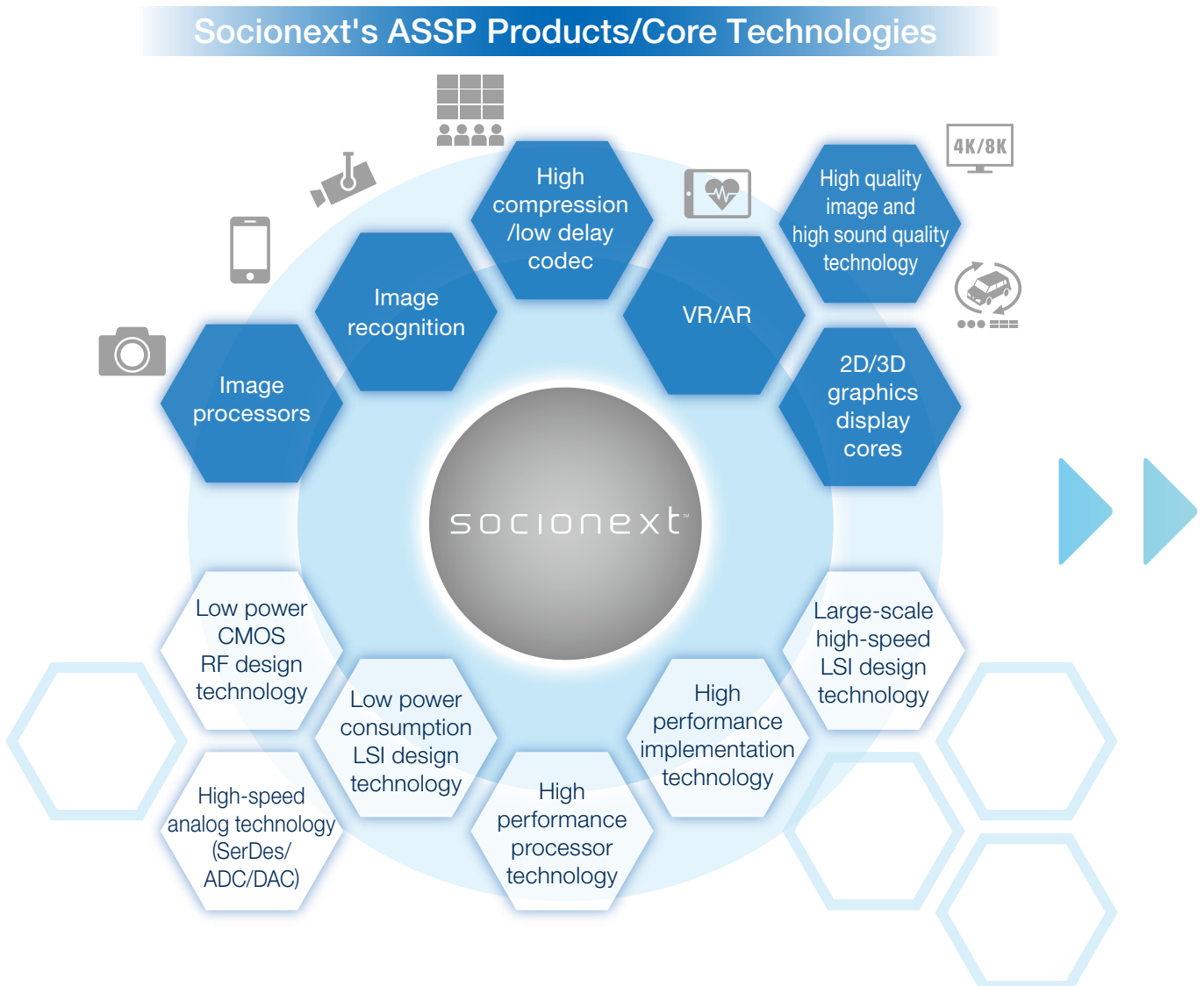
C O N T E N T S
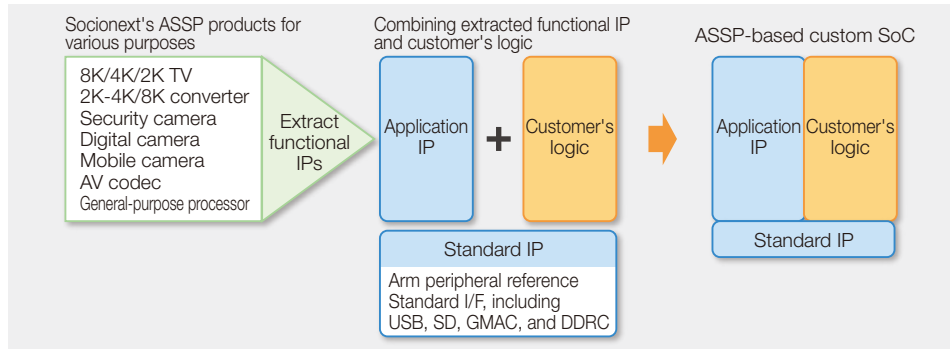
Custom SoC Solution

Reduce Risk and increase added value

Socionext's custom SoC solution reduces the risk and minimize the timescales of new developments.

We support our customers through the complete SoC design process to ensure project success. Previously, the benefits of custom SoC development were often outweighed by increased technical challenges due to the need for higher performance and complexity whilst minimizing power consumption. This led to high development costs and long project timescales.

Socionext's SoC development solution is specifically aimed at addressing these issues, ensuring successful project completion whilst minimizing risk, cost and project duration. In addition to our position as one of the world's leading custom SoC providers, we also offer a wide range of application-specific standard products (ASSPs) to the video- and image-processing, networking and information processing markets. Our ability to utilize design assets from these ASSPs in our customers' SoC projects is a major factor in enabling the development of highly reliable custom SoCs in the shortest possible time – even for new SoC designs. How does this work ? By combining silicon-proven, high value-add functional blocks from our ASSP products with our extensive IP portfolio, we can optimise the functionality of your custom SoC whilst significantly reducing development times and time-to-market for your products.

Socionext's ASSP Products/Core Technologies

High compression /low delay codec

Image recognition

VR/AR

High quality image and high sound quality technology

4K/8K

Image processors

2D/3D graphics display cores

socionext™

Low power CMOS RF design technology

Low power consumption LSI design technology

High performance implementation technology

Large-scale high-speed LSI design technology

High-speed analog technology (SerDes/ ADC/DAC)

High performance processor technology

Custom SoC

## Solution for Development Based on Existing Products

Developing a custom SoC based on an ASSP with a proven track record in the market not only makes it easy to design the components surrounding the CPU and the subsystems. It also has the advantage of easier development and evaluation because related software is also already provided.
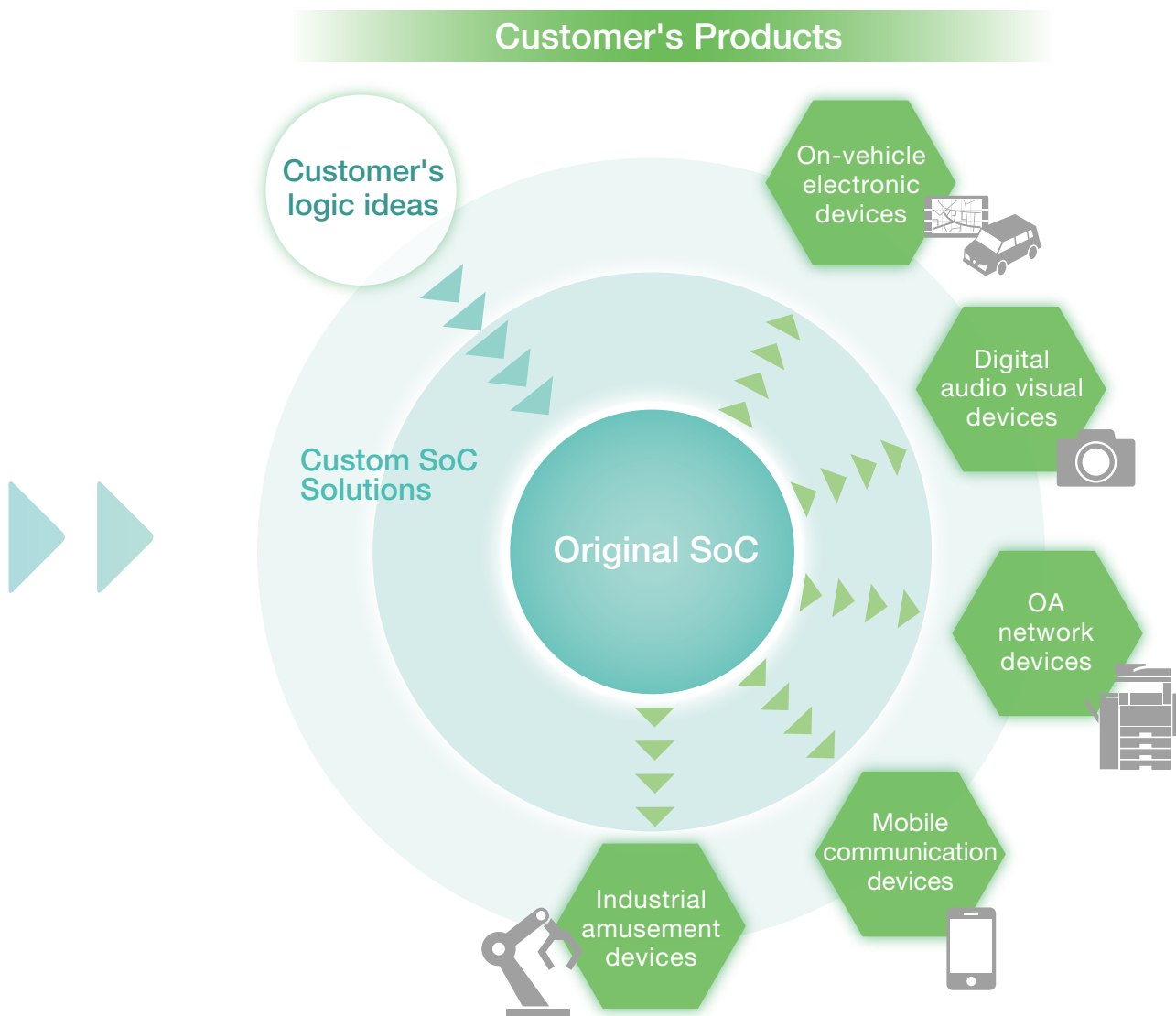
Benefits of ASSP-based Development

Where a product is designed based on our ASSP product, the development period will be six months shorter than that by conventional design. We achieve this rapid time-to-market by shortening the hardware design period for SoC development and by developing software in advance.

- ・Delivery time of sample SoC : Six months ahead of schedule
- ・Advance development of software : Eight months ahead of schedule
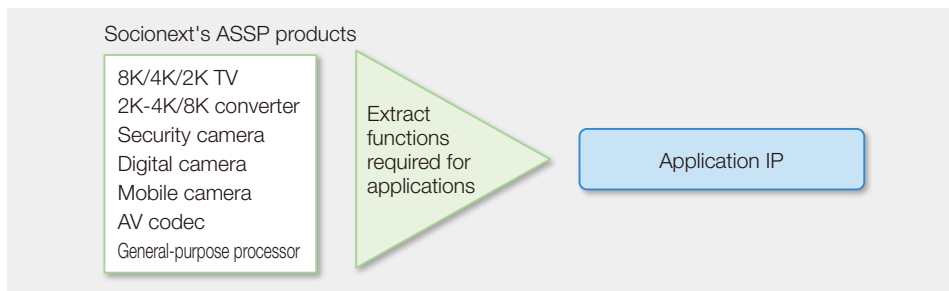- ・Product shipping : Six months ahead of schedule
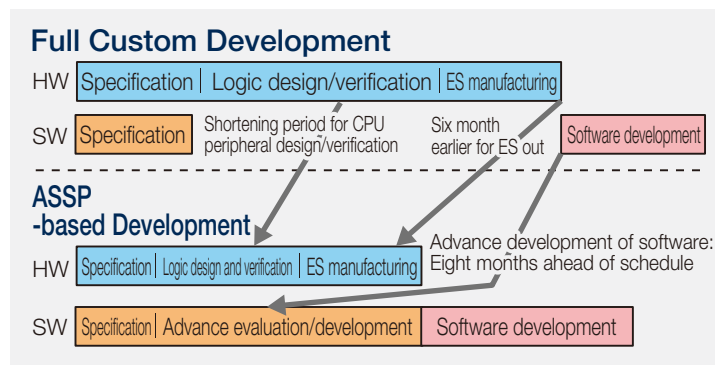
Example of ASSP-based Development

This section introduces one example of ASSP-based development.
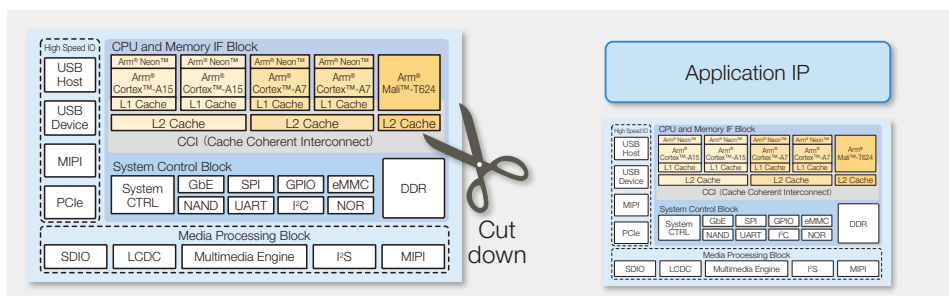
① Extracting necessary application IP from ASSP

We extract application IPs which are required for customer's development from our proven ASSP.

② Combining base platform and extracted application IP

After cutting down unnecessary IPs and Interfaces from base platform, then we combine this optimise platform and extracted application IP.

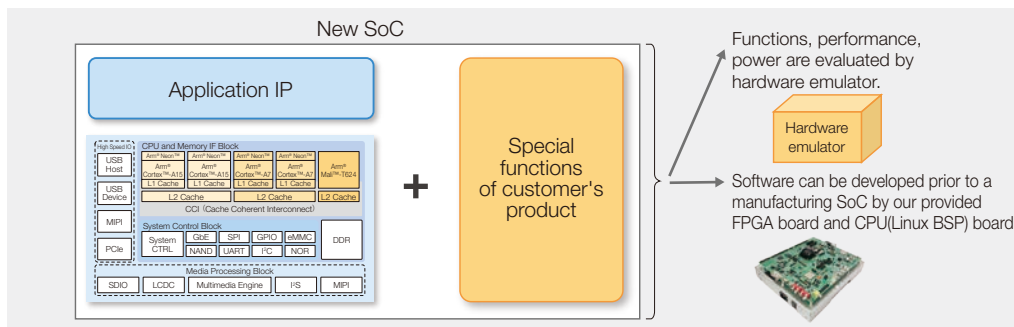③ Adding your special functions to differentiate from others

By adding your special functions to differentiate from others, your special SoC design is now created.

New SoC
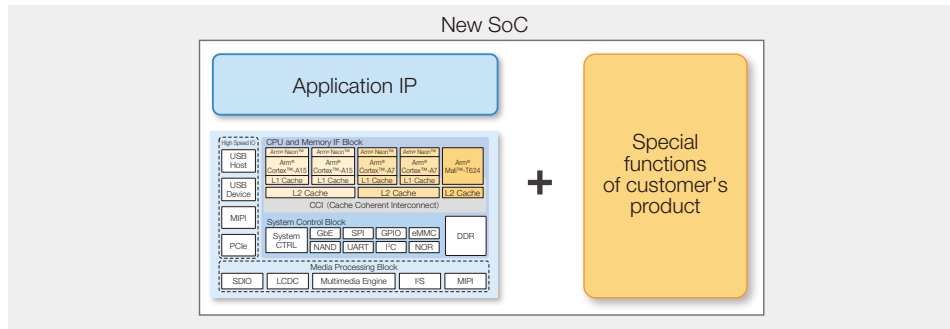
④ Evaluating and verifying functions, performance, and power

The functions, performance, and power can be evaluated and verified using a dedicated hardware emulator at approximately 1000 times as fast as an HDL simulator.

For your software development, we provide a prototype environment such as an FPGA board and CPU board. This allows customers to develop software before manufacturing SoC.

New SoC

Functions, performance, power are evaluated by hardware emulator.

Hardware emulator

Software can be developed prior to a manufacturing SoC by our provided FPGA board and CPU(Linux BSP) board.

⑤ PCB (printed circuit board) co-design

Implementing high-speed components (DDR, PCIe, USB, etc.) and SoC on a PCB tends to cause a electrical issue such as electromagnetic noise, crosstalk, and clock jitter. We analyze such issue creating PCB prototype and offer proposed measures.

This reduces risk associated with developing a PCB and thereby reduces cost for PCB design and manufacturing.
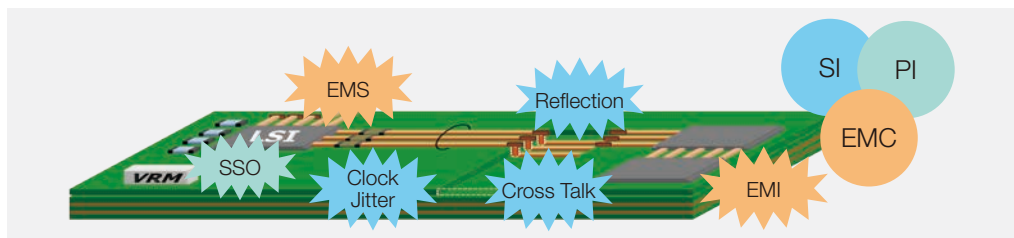
Full Custom Development

To achieve the best performance of your SoC, we have full custom development option that allows you to customize as you like. For your full custom SoC development, we fully support for 1. proposing system architecture, 2. providing subsystem and a various of IPs, 3. optimized CPU peripheral design, and 4. system verification by hardware emulator and FPGA prototype. We also provide a device driver development service under contract as part of our software development support.

Custom SoC Solution Map

At Socionext, we apply an optimized flow according to the features of the SoC to be developed, according to the following design flow.

Standard Design and Development Flow

Planning

Issue definition
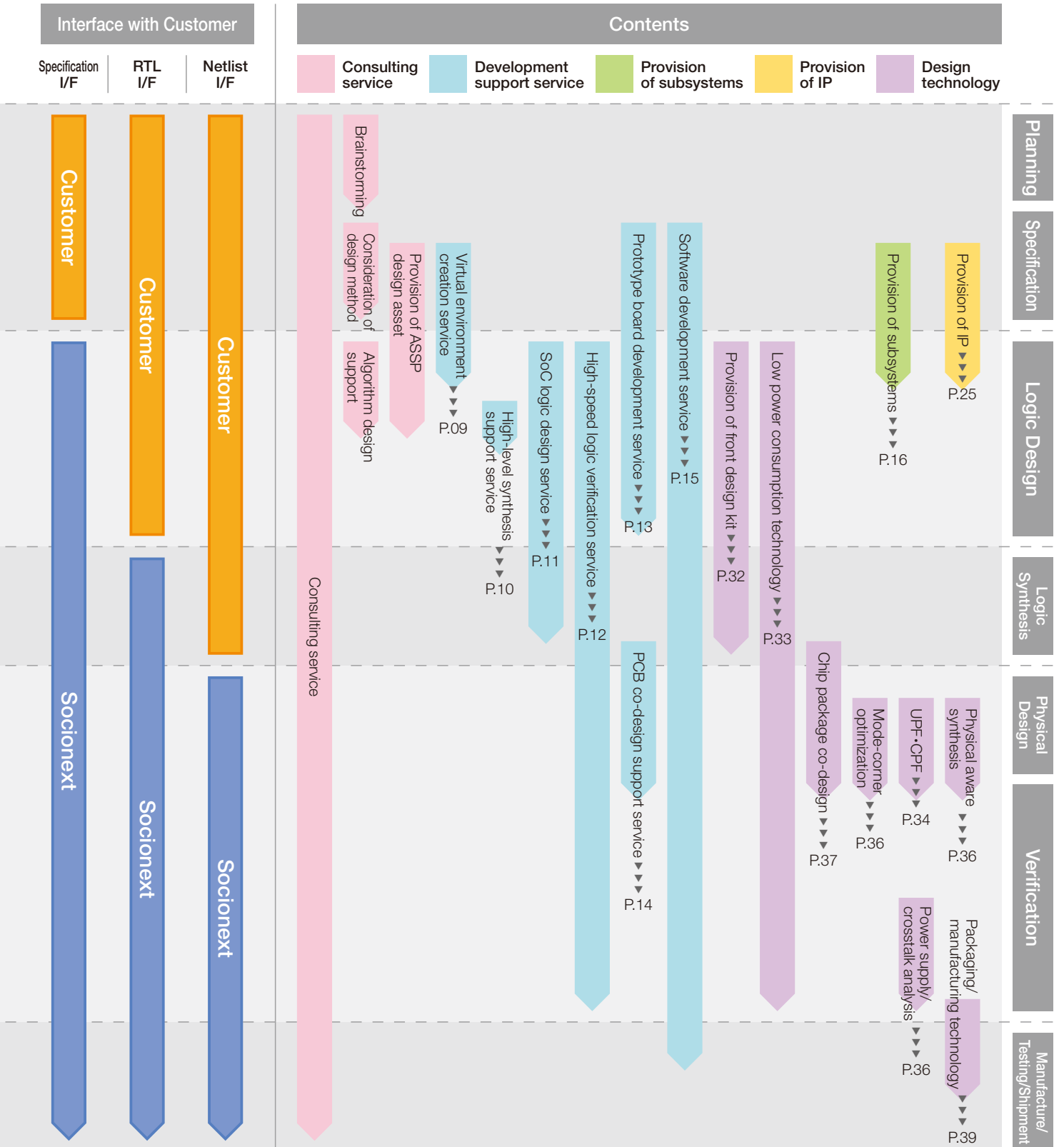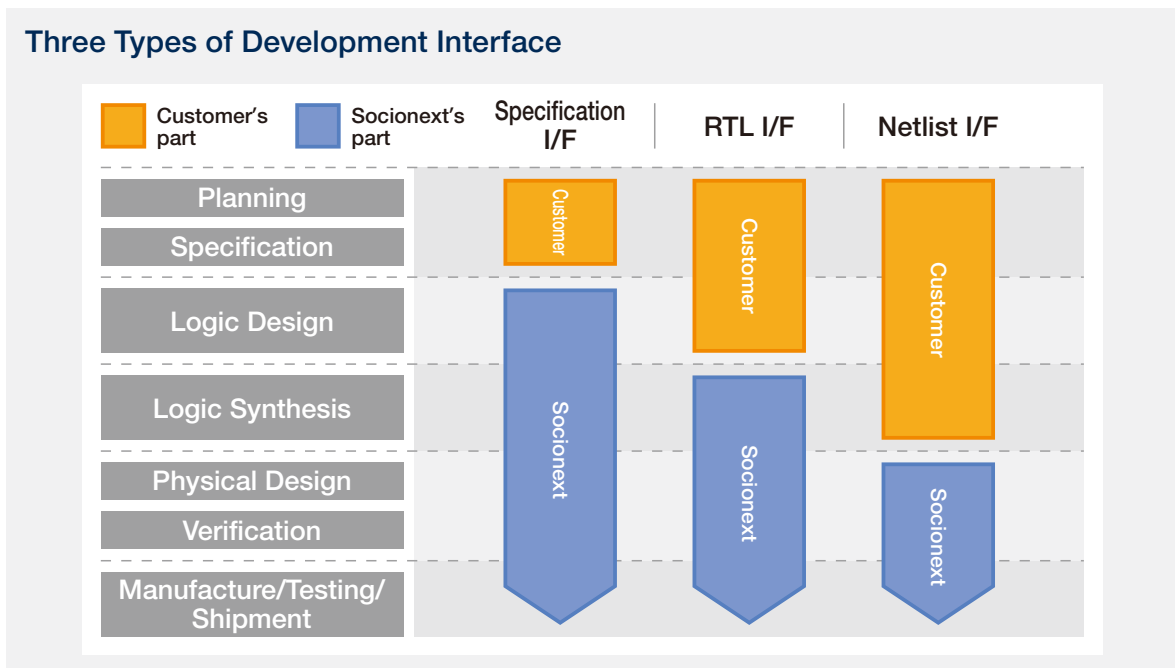
Requirement specification formulation

Development planning

Specification

System-level design

System specification formulation

System-level design

Logic Design

Front-end design

Algorithm design

SystemC rewriting

High-level synthesis

RTL design

Function verification

Logic Synthesis

Logic synthesis

Verification

Physical Design

Back-end design

Design planning

Layout

Verification

Variation timing analysis

Physical verification

Crosstalk noise analysis

Lithography verification

Power rail analysis

Power consumption analysis

Gate simulation

DFT

Test circuit insertion

Test pattern generation

Manufacture/Testing/Shipment

Sign-off

Sample shipment

Mass-production shipment

| Customer's part | Socionext's part |

FPGA prototyping

Board selection/ New development

FPGA fitting

Creating prototyping board

Packaging

Package selection

Package prototyping

Package design

PCB

Specification formulation

PCB prototyping

PCB design

Software design and development flow

Specification formulation

Test design

OS migration
Boot development
Driver development

App development

Creating evaluation board with ES

Evaluating evaluation board with ES

5

Custom SoC

Interface with Customer

Specification I/F	RTL I/F	Netlist I/F

- Customer
- Customer
- Customer
- Socionext
- Socionext
- Socionext

Contents

- Consulting service
- Development support service
- Provision of subsystems
- Provision of IP
- Design technology

Phases: Planning · Specification · Logic Design · Logic Synthesis · Physical Design · Verification · Manufacture/Testing/Shipment

- Brainstorming
- Consideration of design method
- Provision of ASSP design asset
- Virtual environment creation service — P.09
- Algorithm design support
- High-level synthesis support service — P.10
- SoC logic design service — P.11
- High-speed logic verification service — P.12
- Prototype board development service — P.13
- Software development service — P.15
- Provision of front design kit — P.32
- Low power consumption technology — P.33
- Provision of subsystems — P.16
- Provision of IP — P.25
- PCB co-design support service — P.14
- Chip package co-design — P.37
- Mode-corner optimization — P.36
- UPF・CPF — P.34
- Physical aware synthesis — P.36
- Power supply/crosstalk analysis — P.36
- Packaging/manufacturing technology — P.39
- Consulting service

User Interface

Socionext provides the three types of basic design interface shown below. The optimal combination of customers' design assets and our design technologies improves the efficiency of SoC development projects. We also provide a design flow that incorporates upstream verification and FPGA prototyping, supporting ever higher-quality projects and shorter development periods.

Three Types of Development Interface

	Specification I/F	RTL I/F	Netlist I/F
Planning	Customer	Customer	Customer
Specification			
Logic Design	Socionext		
Logic Synthesis		Socionext	
Physical Design			Socionext
Verification			
Manufacture/Testing/Shipment			

Legend: Customer's part (orange), Socionext's part (blue)

・Specification interface
 The specification interface method is used to interface with the customer based on the SoC design specifications. The customer will prepare a design specification document for the SoC to be developed. We will create an SoC development specification document based on those specifications, verify the logic design, and take care of everything right through to delivery of the SoC.

・Interface RTL
 The interface RTL method is used to interface with the customer based on design data (RTL) created by the customer through functional design. The customer will perform functional design through to verifying RTL. We will examine the test specifications, build a test circuit, and manage all processes through to SoC delivery.

・Netlist interface
 The netlist interface method is used to interface with the customer based on a netlist composed of our cells. The customer will perform tasks up to logic synthesis for netlist creation.

Development Support Service (DesignExpress™)

Development Support Service (DesignExpress™)

This design service provides you with consistent development support for everything from system specification to evaluation, as well as for PCB design, in every facet of custom SoC development. This service enables you to focus on your product development while shortening the development period, reducing risks associated with reworking, improving product quality, and reducing power consumption.

List of Development Support Services

- Virtual environment creation service (Cedar™-ESL)
- High-level synthesis support service (Cedar™-HLS)
- SoC logic design service
- High-speed logic verification service (Cedar™-EMU)
- Prototype board development service (Cedar™-PROT)
- PCB co-design support service (PLACATE™)
- Software development service

Virtual environment creation service (Cedar™-ESL)

When considering SoC specifications and architecture, you only need to choose the services you actually need. Select from the following four menu items from the virtual environment creation service.

- Virtual environment creation service for feasibility studies
- Environment for measuring detailed bus architecture performance + Performance evaluation
- Environment for advance development of software
- Environment for software-driven performance evaluation

Advance development of software
- Software development

SW
| CPU | DMA | IP |
| BUS |
| MEM | TIM | IRC |

Determine software architecture, IPs to use, memory mapping, and data flow

Software driven performance evaluation
- Rough architecture design
- Use case extraction

SW
| CPU | DMA | FPGA (RTL) |
SCEMI-I/F
| Cross Bar |
| MEM | BUS |
| TIM | IRC |

Determine bus width, frequency, bus architecture

Architecture performance evaluation
- Detailed architecture design

SW
CPU	DMA	IP
MEM	BUS
TIM	IRC

Determine detailed configuration, cross-bar and number of FIFO stages.

Service Category	Service Description	Item Submitted by Customer	Deliverable from Socionext (Example)
Provide of development environment for advance development of software	A virtual platform for software development is provided	Block diagram Block functional specification	High-speed virtual platform (for software development)
Provide of environment for software driven performance evaluation	A virtual platform for software driven performance evaluation is provided	Block diagram Block functional specification Software scenario	High-speed virtual platform (for architecture design)
Provide of environment for detailed architecture performance evaluation	A virtual platform for architecture performance evaluation is provided. Performance is measured	Architecture construction diagram Evaluation scenario	High-accuracy virtual platform Performance measurement report

High-level synthesis support service (Cedar™-HLS)

The high-level synthesis support service rewrites source code and provides a library that can be synthesized with that code. This tunes your source code into a high-level language (SystemC/C/C++) for adaption to the applicable process technology. After checking the consistency between the high-level synthesis results and the process technology to be used, we provide you with rewritten source code and the like.

Cedar™-HLS Service Outline

Customer's tasks	Socionext's tasks

Algorithm C/C++

Specifications, test bench

Cedar™-HLS service

High level synthesis optimization/verification

Code, high level synthesis constraints, verification report

Performance report option (Timing)

High level synthesizable C/C++

Verification/high level synthesis

Provided

Library

RTL Rule Set

RTL

RTL Style Check

RTL hand-off

RTL Style Check

Logic synthesis

Logic synthesis

Equivalence verification

Netlist

Netlist hand-off

Netlist

Placement and routing

Placement and routing

Service Category	Service Description	Item Submitted by Customer	Deliverable from Socionext (Example)
Handing off of RTL designed with high level synthesis RTL hand-off	Rewriting of a language in accordance with the tool Rewriting of a language in accordance with constraints	Functional specifications Constraint conditions High level language	Rewritten high level language Library for high level synthesis RTL designed with high level synthesis

Development Support Service

SoC logic design service

With the SoC logic design service, Socionext will do the logic design on your behalf. In addition to complete SoC design, we can also do partial design. By combining various functional macros that we handle, we provide design data that best suits your system. Note that design data includes a functional specification document, RTL, and a verification report.
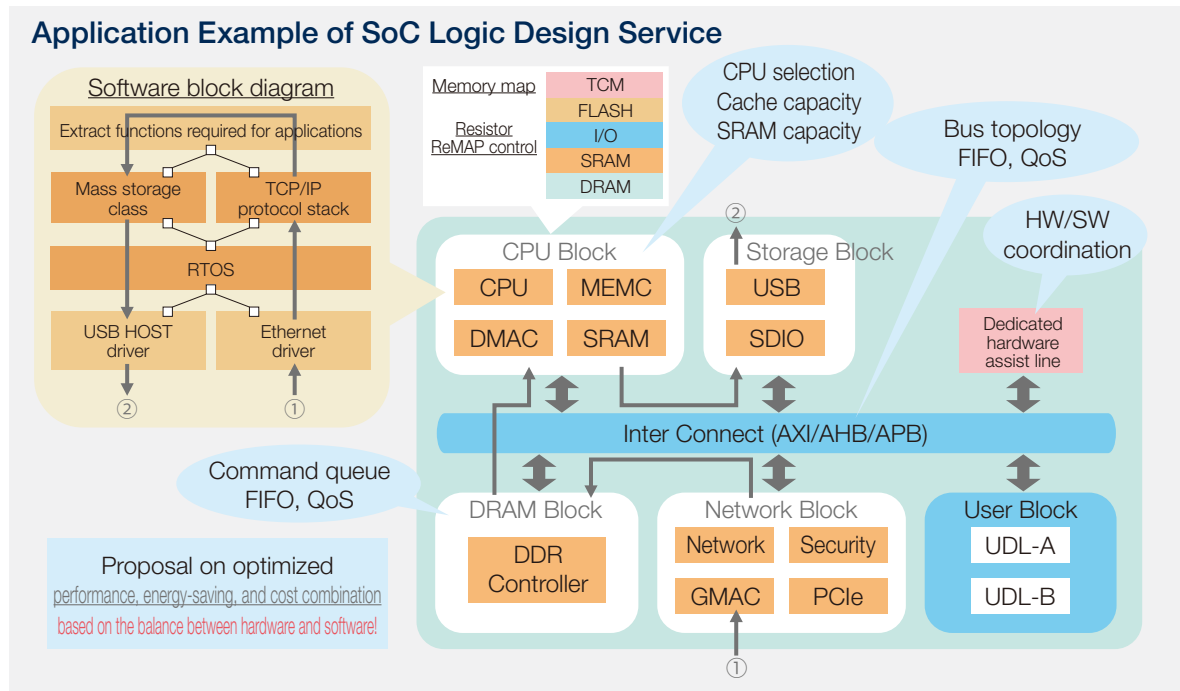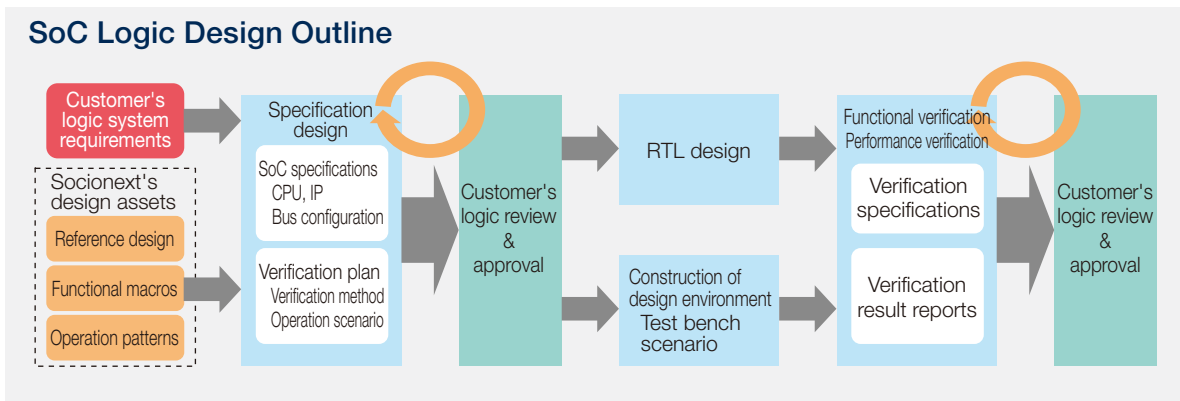
SoC Logic Design Outline

Application Example of SoC Logic Design Service

Service Category	Service Description	Item Submitted by Customer	Deliverable from Socionext (Example)
SoC Logic Design	Specification design	Requirement specifications Macros to be installed Use cases Functional and performance requirements	SoC specifications
	RTL design		RTL
	RTL verification		Verification specifications,result reports

High-speed logic verification service (Cedar™-EMU)

The high-speed logic verification service uses emulators and the like to perform high-speed logic verification and compute SoC power consumption. We can prototype a circuit by mapping a circuit of the system to be developed to an emulator. It can also compute your proposed system's power consumption. Since the emulator runs 500 to 1,000 times faster than a software simulator, you can significantly reduce verification time.

Cedar™-EMU Service Outline

＜Simulation environment＞

Created with

CPU, etc. Simulator (ISS)

design RTL

①Formulation of verification specifications
②Construction of verification environment

Software (Created with Cedar®-ESL)

Verification data

③Preparation of verification data

＜Emulation environment＞

Created with

design RTL

CPU, etc. Actual chip

Input RAM

Output RAM

④Verification

Verification data

Result collection

Software debugging with ICE
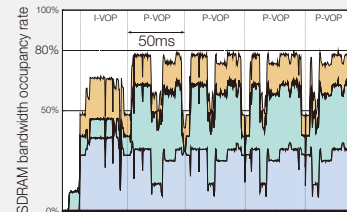
Performance analysis with bus monitor
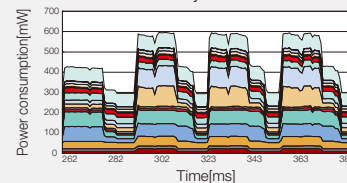
Power consumption analysis

Service Category	Service Description	Item Submitted by Customer	Deliverable from Socionext (Example)
Chip level verification	Formulation of verification specifications Creation of verification data Construction of verification environment verification	Outline block diagram Design data (RTL or netlist) Input/expected value data	Verification specifications Verification data Emulation verification results
System level verification	System level verification using software developed in an ESL environment	Design data (RTL or netlist) Input/expected value data Test programs	Emulation verification environment Verification result reports
Power consumption reduction	Measurement of power consumption	Power measurement program	Reports on results of power consumption measurement

Development Support Service

Prototype Board Development Service (Cedar™-PROT)

The prototype board development service provides a prototype board for system-level verification and advance development of software. By implementing an IP equivalent to the IP to be installed on the system on an FPGA, this service provides a board that is equivalent to the target system. Since we can perform system-level verification and advanced software development before the SoC is completed, you can improve its quality and shorten the development period.

Software development technology
IP verification with implemented driver
Software platform can be provided

Board design technology
Printed board design supporting high-speed interface

System development that enables verification on actual equipment

High equivalence with custom SoC
Prototype development using custom SoC IP

Arm core can also be implemented

Custom SoC/FPGA design technology
Logic design based on presented specifications

ROM
RAM
Arm (EVA chip)
FPGA (Custom SoC IP)
FPGA (User)
Custom SoC
I/F

Record of applications of Cedar™-PROT
· Controller custom SoC for network
· Custom SoC for measuring instruments
· Image processing custom SoC for documents
· Many others

Semi-custom board
FPGA prototype board

Service Category	Service Description	Item Submitted by Customer	Deliverable from Socionext (Example)
System level verification	Provide of a prototype board	Requirement specifications (specified circuit information,etc.)	Board unit Board specifications FPGA ROM data

PCB Co-design Support Service (PLACATE™)

The PCB co-design support service analyzes noise and supports countermeasures based on an integrated SoC and PCB model that help you to significantly shorten the system development period and reduce costs through reduced BOM.
By applying this service from the upstream phase of custom SoC design and PCB design, we help to cut your design time by reducing the amount of SoC and PCB design rework that needs to be done, thereby improving their systems and significantly shrinking the evaluation workload.

Design Flow Image

・Identification of issues through integrated CHIP-PKG-PCB analysis
・Feedback to CHIP-PKG-PCB design

・Easy difference analysis when changing components
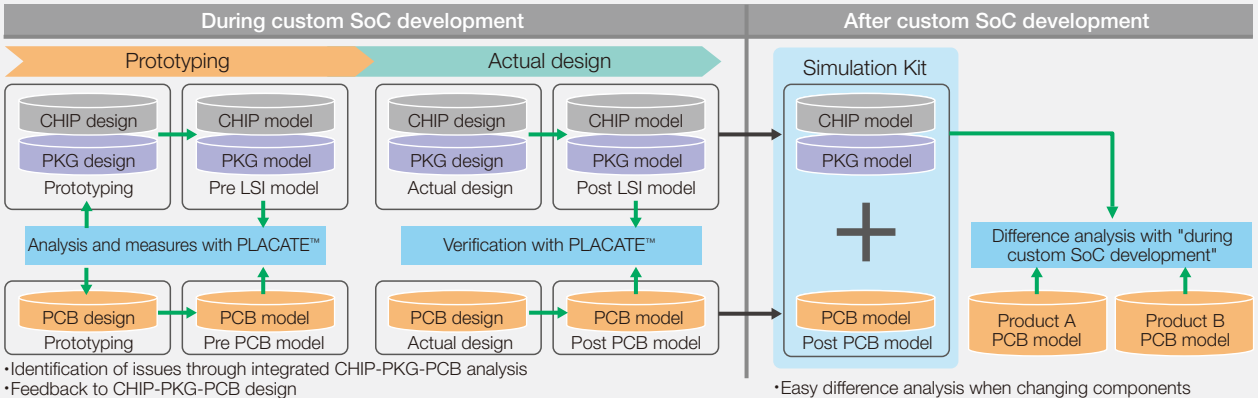
Service Description	Deliverable (Example)
■ Board prototyping ・Wiring/Reducing bypass capacitors ■ Integrated noise analysis for SoC, PKG, and Board ・DRAM-IF (DDR4, etc.) SI/PI analysis ・SerDes (PCIe Gen3, etc.) SI analysis ■ Creation of SoC power supply models ・LPM+IBIS5.0 ■ Looking into measures for EMC ・Consulting by iNARTE engineers	Board design guidelines Board reference design SI/PI analysis result reports SoC power supply model (LPM+ IBIS5.0) EMI analysis results EMI countermeasure proposals

Structure of Simulation Kit
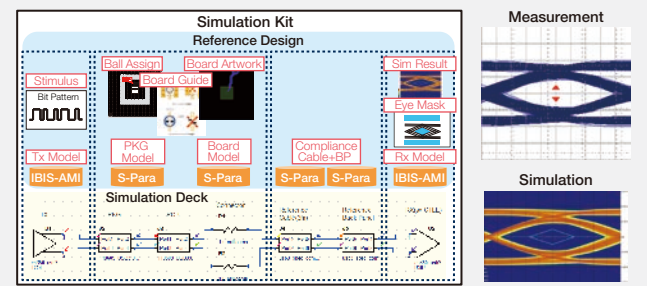
Case of Bypass Capacitor Reduction

Confirmed that capacitors can be reduced by up to 25% of the initial proposal based on the integrated chip-package-PCB verification
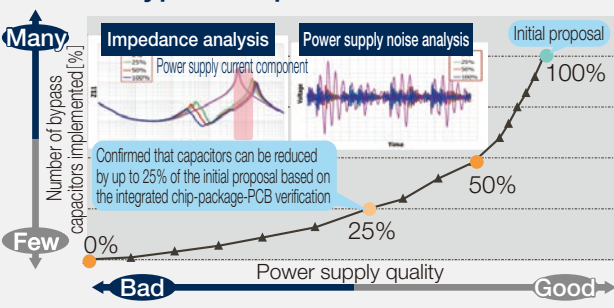
Case of EMI Analysis

Near Field

Far Field
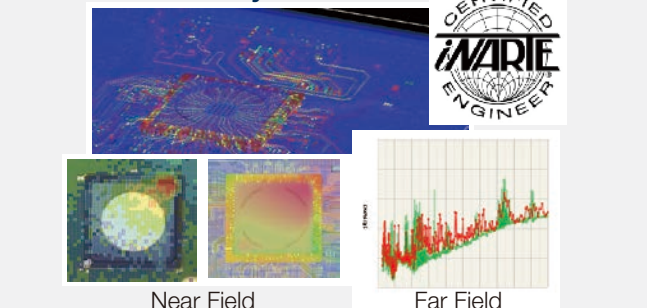
Software Development Service

When reviewing the hardware specifications, it is important to examine the factors that form the basis of your SoC, such as the system startup sequence and power-saving features. Also, after deciding on the specifications, these need to be embodied in software and checked in terms of the logic verification and board verification phases. Socionext works with you during such phases from the perspective of software development, and supports you in specification design through to board evaluation. All this produces a system that is consistent across hardware and software, ensuring reliability.
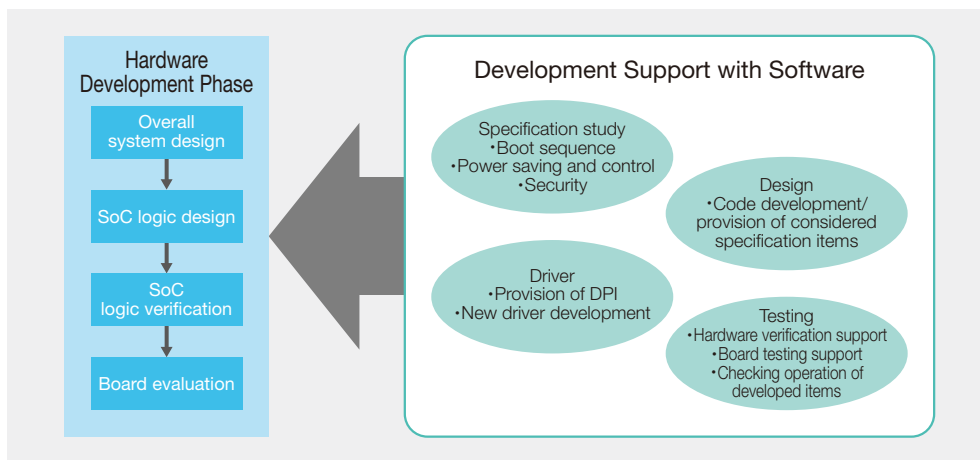
[Software Development Service]

●DPI (Device Programming Interface)

DPI is an IP operation sequence in which a group of functions, including initialization, starting operation, and stopping an IP macro, is written into software, and for which the operation check has been completed. You can use DPI in various development phases in the following ways:

- To check IP operation at an early stage (to be reflected in hardware verification scenarios)
- To develop device drivers in a short time (assisting the user in understanding specification documents, use of API)
- To quickly evaluate engineering samples (IP communication check, analysis)

●Subsystems

Various types of subsystem are available for use as the foundation for support services. For details, see the section on subsystems.
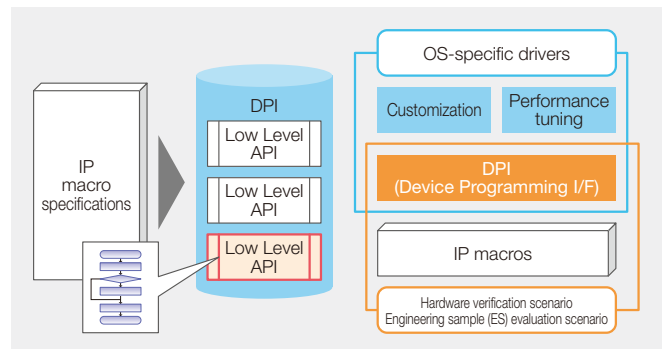
Examples of Development Support Services

Category	Service Details
Boot	・Support for considering boot-sequence specifications ・Boot code design ・MAIN system startup-code design ・Secure boot-development support 　・Proposal on secure boot sequence 　・Secure boot implementation 　・Secure boot-operation check support
IP driver	・Providing DPI for Socionext IP
RTOS support	・OS migration support ・Operation check support for provided drivers
Power saving	・Power-saving code design ・Providing and embedding network standby response code

Subsystem Service

Provide of Subsystems

Socionext provides subsystems featuring specific functions enabled by combining various types of IP. By incorporating a subsystem, the main system can achieve high performance with a specific function and low power consumption.
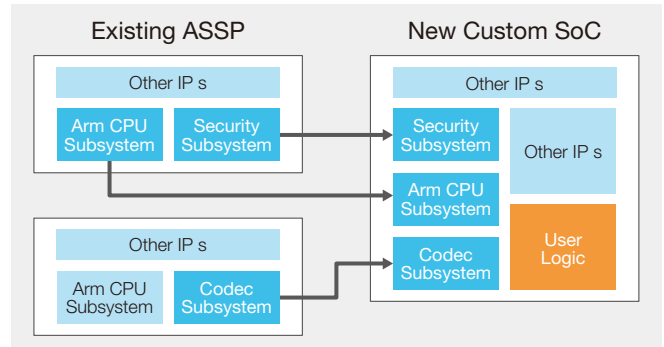
Image Signal Processor Subsystem

● Background and Initiatives

Under the current circumstances where camera solutions continue to advance, it is extremely difficult to keep providing new functionality and offering differentiating features every year.

We have created IP for the image macro part of our image signal processor (Milbeaut®) with a track record of 18 years and provide it as a high-resolution, high performance subsystem.

● Outline

By creating IP for an image macro for each functional block, it is possible to build a flexible platform. Each IP has the AXI interface so SoC integration is easy.

● Features

- High-performance 4Kp60 600Mpix/sec (ex TSMC 28nm HPC+)
- API for effectively using image macros is provided.
- An image adjustment simulator is provided to emphasize the individuality of images.

Lineup

| IP Block	Function	
B2B	Bayer domain processing	Noise reduction, resizing, defective pixel correction, 3A (AE/AWB/AF) statistics, shading correction
B2R	Demosaic processing	White balance gain, color interpolation
LTM	Local tone mapping	Local tone mapping
R2Y	RGB to YUV conversion	Color correction, tone correction, gamma correction, multi axis color correction, YUV conversion (444/422/420), edge enhancement luminance noise reduction, resizing, Y histogram
CNR	Color noise reduction	Color noise reduction, purple fringing correction
3DNR	Multi-frame noise reduction	Noise reduction with reference to multiple images
HDR	High dynamic range synthesis	Dynamic range expansion by synthesizing two different exposure images
LDC	Lens distortion correction	Correction of image distortion caused by optical characteristics

Low light intensity noise reduction
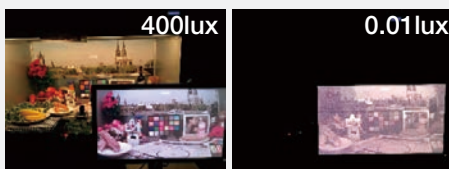
Defective pixel correction

Lens distortion correction
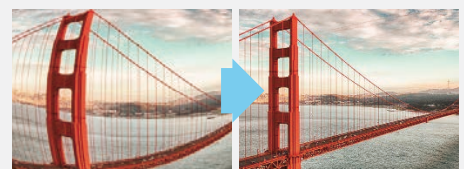
Arm® Processor Core Subsystem

Arm Cores and Design Kits

The comprehensive license agreement with Arm allows customers to select the most suitable Arm core to meet their requirements. We provide the most suitable Arm core and SNAP-DK (design kit), a design environment, for custom SoC for a wide range of applications such as microcontrollers, embedded device, and application equipment.

These Arm Cores in the line-up are available on all process technologies that Socionext offers.

Socionext Arm Platform (SNAP)

Use of the SNAP (Socionext Arm based SoC Platform) reduces development time and risks in Arm core-based SoC development. SNAP consist of the following.

●Design Kits: SNAP-DK, ADK, SDK
- SNAP-DK : Consists of an Arm core and minimum required peripheral IPs.
- SNAP-ADK : SNAP-DK-based design kit that al-ready implements an interface macro, GPU, etc.
- SNAP-SDK : This design kit provides a fully customized dedicated subsystem for customers using a design tool in accordance with the requirement specifications.

By selecting the most suitable design kit based on the specifications customers require, development time can be reduced significantly.

These design kits, containing a simulation environment, test bench, sample boot code, etc., contribute to the shortening of time to launch the design environment and creation of an appropriate Arm core boot program.

●Prototyping: SNAP-PK
- The SNAP-PK provides Socionext's unique FPGA board with SNAP-DK. By implementing a user logic on the FPGA side, it achieves prototyping of an SoC.
- This product can be used for system operation verification of hardware, performance evaluation, and early development of software.

Line-up of Arm Core, GPU and SNAP-DK

Arm core			
Arm v4,v5,v6	Arm v7	Arm v8	
●Arm11	●Cortex-A		○Cortex-A75/A73
●Arm9	●Cortex-R	●Cortex-A72	○Cortex-A55
●Arm7	●Cortex-M	●Cortex-A53	○Cortex-A35
GPU			
Utgard	Midgard	Bifrost	
●Mali-400	●T820		○G71
	●T620		○G51
SNAP-DK			
●DK-11	●DK-Av7	●DK-Av8(A53)	○DK-Av8
●DK-9	●DK-Rv7		DK-Rv8
●DK-7	●DK-Mv7		○DK-Mv8

●available　○planning

SNAP Design Kits

Type	Content	Advantage
SNAP-DK (Basic Design Kit)	CPU + small-scale peripheral IPs	Bootable CPU subsystems can be used
SNAP-ADK (Advanced Design Kit)	SNAP-DK + high performance IPs (system with guaranteed performance)	High performance CPU subsystems including an OS can be used
SNAP-SDK (System Design Kit)	Consultation-based full custom design kit (system with guaranteed performance)	Dedicated subsystems based on requirement specifications and existing systems can be used

SNAP-PK

(Example) SNAP-DK-M3 ＋ Customer's logic

Semi-custom board
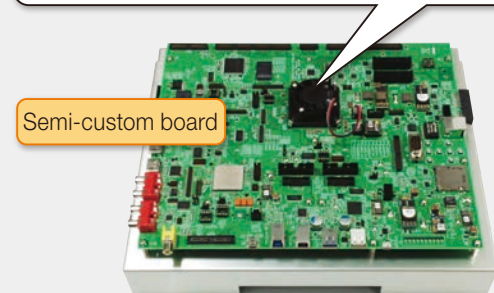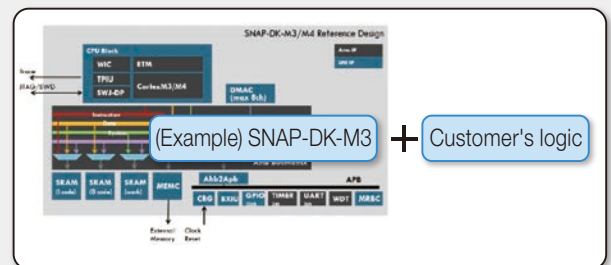
Video Codec Subsystem

● Background and Initiatives

Due to an imbalance between the advance of DDR memory to the ultra-high speed generation along with an increase in the burst length and access by video codec processes handling small size rectangular image data to the DDR, a reduction in the efficiency of using the DDR memory band width has become an issue. This subsystem enables high efficiency video codec processing that can save the band width using Socionext's unique technology.

● Outline

We have developed our unique bus protocol methodology that can improve memory access efficiency in the codec process without being significantly affected by advances in DDR.

Tightly coupling our codec engine and our memory controller with the methodology enables the memory controller to efficiently access DRAM by taking into account a physical memory map based on the 2D information on image data accessed by the codec engine, reducing the required memory band width significantly.

● Features

· Achieves various types of HEVC codec processing with a smaller bus width (bit) as listed below.

Example: When using LPDDR4 2400 Mbps

	Processing details	Socionext's conventional system	Video codec subsystem
Decode	4k 60p 4:2:2 10bit	112bit	64bit
	4k 60p 4:2:0 10bit	96bit	48bit
	4k 60p 4:2:0 8bit	64bit	32bit
Encode	4k 60p 4:2:2 10bit	96bit	48bit
	4k 60p 4:2:0 10bit	80bit	48bit
	4k 60p 4:2:0 8bit	64bit	32bit

General Relationship between Codec IP Core and DDR Memory

Codec engine

General-purpose bus

Y position
X position
Y size
X size

Information regarding 2D data is lost

Bank 0 | Bank 1

Memory controller

Bank + Physical address

12 commands

Bank 0 | Bank 1

DDR memory **Frequent small memory access**
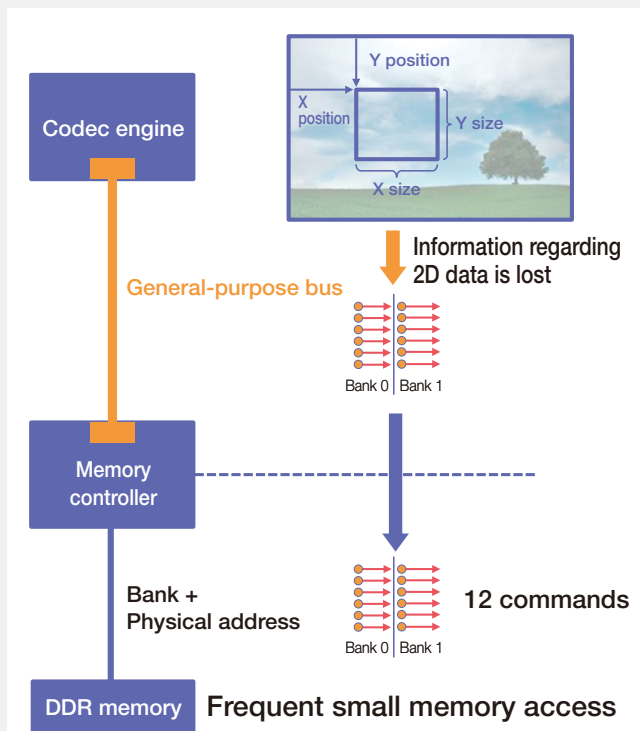
Relationship between Socionext Codec IP Core and DDR Memory

Socionext's Codec engine

Socionext's unique bus protocol

Y position
X position
Y size
X size

(1) Access with a large rectangular size by taking into account memory access efficiency
(2) Sharing of information on 2D data between the Codec IP and memory controller

Socionext's Memory controller

Logical -> Physical conversion

Bank + Physical address

2 commands

Bank 0 | Bank 1

DDR memory **Efficient memory access**

IP Video Streaming Subsystems

●Background and Initiatives

With the spread of the Internet, demand for video streaming is exploding. Typical examples are media servers for downstreaming and network monitoring cameras for upstreaming. In such target areas, Socionext carries out fragmentation and IP packetization of video data after codec processing, significantly reducing the processing load of the main system.
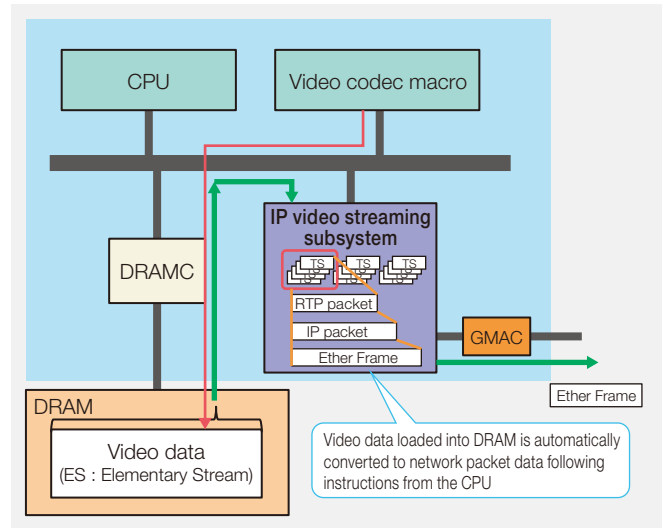
●Outline

This subsystem encapsulates video and audio data into an IP packet and encapsulates the IP packet into an Ethernet frame. The high-performance IP macro executes the following series of processes just by placing data after codec processing.

- Packetizing video data (ES: elementary stream, loaded into DRAM) into TS packets
- Encapsulating ES, TS, or JPEG data into RTP packets
- Encapsulating RTP packets into IP packets
- Encapsulating IP packets into Ethernet frames and performing GMAC control (video transmission)

●Features

- Support for RTP/UDP offloading
  [Supported formats]
  - ES over RTP: Video (H.264), Audio (G.771, AAC)
  - JPEG over RTP
  - TS over RTP
  - Metadata over RTP
- Support for Max. 32 streams
- Integration with security (encryption) functionality

Video data loaded into DRAM is automatically converted to network packet data following instructions from the CPU

Transfer band (Mbps)	10	30	50	150	300	500
Offloading not available CPU load factor (%)	23	62	100			
Offloading available CPU load factor (%)	-	-	15	21	29	39

Load reduced by 25 times

Actual measurement of products

HDMI 2.1-Compatible Data Transmission and Reception Subsystem

● **Background and Initiatives**

The HDMI 2.1 specifications were defined in 2017. It has 48-Gbps bandwidth, 2.7x that of conventional HDMI 2.0, and enables the transmission of extremely large data sets, including 8K video, with very low latency while maintaining high image and sound quality. With our extensive knowledge in developing of data-transmission technologies for consumer video equipment such as recorders and 4K TVs, as well as for high-speed, serial data transmission used in large-scale servers, Socionext offers the world's first HDMI 2.1 compatible data transmission and reception subsystem (Link/PHY).

● **Outline**

This subsystem supports the HDMI 2.1 (High-Definition Multimedia Interface) specification. It supports video resolution of up to 4320 x 7680p and color depth of 8, 10, and 12 bits, and covers a bandwidth of 48 Gbps. While supporting L-PCM audio data and compressed audio data, the subsystem supports high bit-rate audio (up to 768 kHz) as well as sampling rates from 32 kHz to 192 kHz.

● **Features**

- ・Support for VESA DSC 1.2a
- ・Support for Dynamic HDR and eARC
- ・Support for game mode VRR/QMS
- ・Support for HDCP2.2
- ・Support for hot plug detection

[Example: HDMI 2.1 Receiver PHY/Link]

LINK

SNIHSKHD21RX1T28PNSV0

Pixel Clock
FRL Clock
Data0[35:0]
Data1[35:0]
Data2[35:0]
Data3[35:0]
Data Enable
HSYNC
VSYNC

Video Data

HDMI Core

HDMI PHY

CH0 Data/TMDS ch0
CH1 Data/TMDS ch1
CH2 Data/TMDS ch2
CH3 Data/TMDS Clock

Meta Data/Packet Data — Meta Data / Packet Data

DDC

Master Clock
SPDIF
I2S[15:0]

Audio Data

HDCP Engine

HDCP Key

OTP ROM

Register Access (APB Bus) — Register
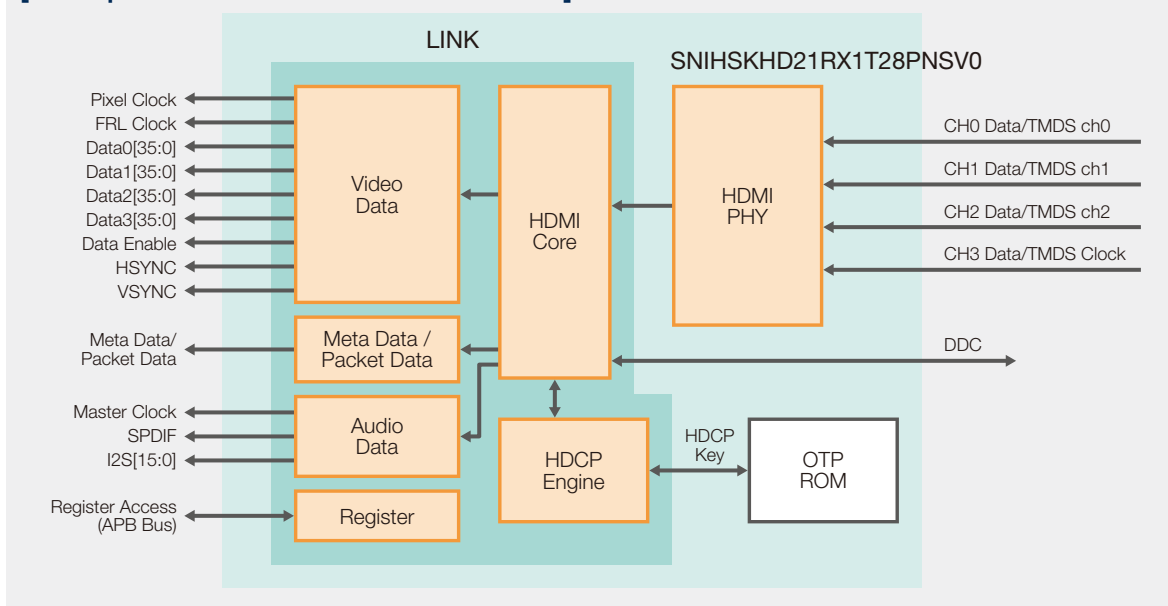
Power-saving Subsystem

●Background and Initiatives

In step with SoCs becoming more functional and highly integrated recently, providing a power-saving mode has become an absolute essential. For example, network standby mode keeps the minimum required interfaces, mainly network functions, awake and places the remaining functions in standby to save power. Sleep mode keeps only subsystems awake to make the system enter a deeper sleep, and there are various ways to implement power-saving mode. We provide a power-saving system to satisfy such needs.

●Outline

A power-saving subsystem is composed of an Arm microcomputer, minimum required peripheral IP, RAM, and others, and operates separately from the main system. By doing so, this subsystem allows you to achieve the following functions.
- ・Transition and return from power-saving mode with a simple instruction from the main system to the subsystem
- ・Achieve deep-sleep mode by keeping only the subsystem awake
- ・Integrate the power-up and shut-down sequences
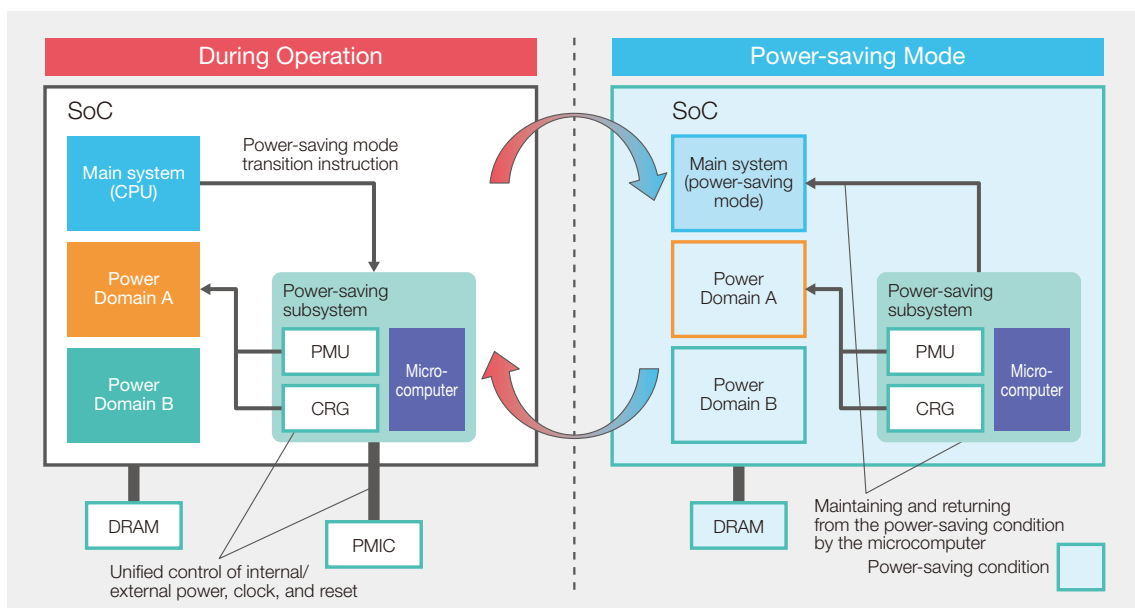
We offer the following support services that make it easy to introduce the subsystem.
- ・Support for considering system power-saving sequences between the main system and subsystem
- ・Software design support for main system sleep and wake-up scenarios
- ・Design support for controlling the subsystem power supply

Network Standby Response

Network standby response is a function in which the subsystem carries out packet processing on behalf of the main system when it is in a standby state. This function also supports the following functions.

[Supported functions]
- Main system wake-up assistance when a packet requiring processing by the main system is received
- The acceleration function that accelerates packet processing in a normal state

Network Standby Response Outline

SoC

Main system
- CPU (x n) (AP)
- DMAC
- User Logic1
- MEMORY Ctrl.

Power-saving subsystem
- CPU (microcomputer)
- SRAM
- GMAC
- PHY

Standby response FE

Always-on power supply ON

During normal times:
Provides a network acceleration function from the standby response FE

During system standby:
Maintains network functionality by using the subsystem's firmware

Actual Network Standby Response Performance Values

Function/Performance	Normal	When using proprietary technology	Comparison
Stand-by power	2 W to several W	<100mW	<1/20
Communication performance	300Mbps	900 Mbps (20% reduction in CPU load)	Approx. 3 times

Actual measurements with MB86S73 board

Security Subsystem

●Background and Initiatives

With the recent progress of the IoT (Internet of Things), a security system has become an essential item. Although a high level of protection for secret information and high-speed algorithm processing by hardware are indispensable for a security system, it is not easy to develop such hardware and software from scratch. Using Socionext's security subsystem can reduce the burden of such development, making it possible for you to introduce a security system efficiently.

●Outline

The security subsystem includes a dedicated key storage box to store highly secret key information. It also incorporates a hardware engine that uses the stored key to perform high-speed encryption and authentication processing, achieving a high-level security system.

[Features of the security subsystem]
①Secure key generation and input through a dedicated e-mail box
②Secure key storage through locating key storage in a module
③A dedicated engine that uses a key in a secure key storage box

The following presents an example function using this subsystem and system configuration.

● Example Function Using Subsystem: Secure Boot

The boot code is executed at the beginning of system startup, and whether a correct program is used or not must be examined on the basis of the boot code. It is the key for a security system where such important code is encrypted and stored, and a mechanism is in place to detect whether such code has been altered. The security subsystem provides a mechanism to protect and securely execute such important code.
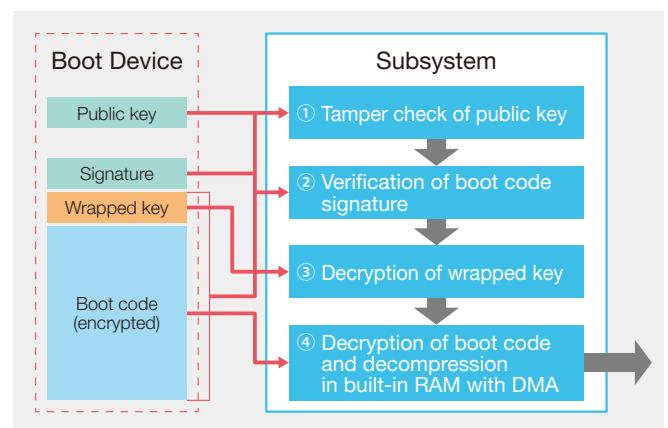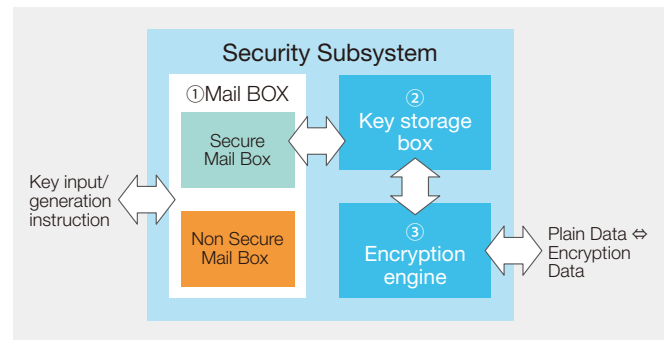
● Example of System Configuration Using Subsystem

The security subsystem can be applied as follows for the entire system.

① Secure boot from a micro computer in a secure sub-block and ROM

② Creation of a dedicated key storage route and encryption processing for a non-secure main block

③ Key management for another encryption engine by using the security subsystem and a microcomputer in a secure sub-block
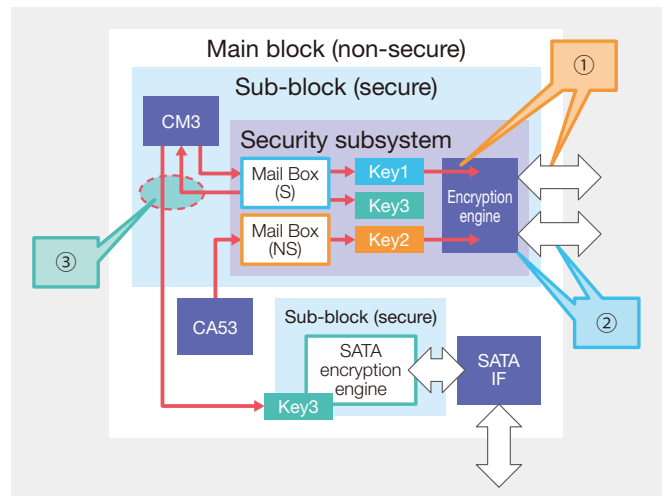
● Hardware Accelerator

The following shows a list of security algorithm accelerators installed in the subsystem.

System		Key Length (bit)
Common key encryption	3DES-ECB	168
	3DES-CBC	168
	AES-ECB	128/192/256
	AES-CBC	128/192/256
	AES-CTR	128/192/256
	AES-GCM	128/192/256
Hash	SHA-1	–
	SHA-256	–
	SHA-512	–
HMAC	SHA-1	160
	SHA-256	256
	SHA-512	512
Electronic signature generation/verification	RSA	2048 - 3072
	ECDSA	256/384/521

IP Macro Service

Line-up of IP Macros

Socionext's IP macros with their proven track records support customers in advanced SoC development.

●Functional/Interface Macros

Category	Function	Process Technology					
		90nm	65nm	55nm	40nm	28nm	16nm/12nm
Arm Cores	Cortex-A	✓	✓	✓	✓	✓	✓
	Cortex-R	✓	✓	✓	✓	✓	✓
	Cortex-M	✓	✓	✓	✓	✓	✓
	Arm11, Arm9, Arm7	✓	✓	✓	✓	✓	✓
	Mali	✓	✓	✓	✓	✓	✓
Image Core	JPEG	✓	✓	✓	✓	✓	✓
	H.264	✓	✓	✓	✓	✓	✓
	H.265	✓	✓	✓	✓	✓	✓
Security Core	SHA	✓	✓	✓	✓	✓	✓
	PKA	✓	✓	✓	✓	✓	✓
	3DES	✓	✓	✓	✓	✓	✓
	AES	✓	✓	✓	✓	✓	✓
Interface Controller Core	OSPI/QSPI	✓	✓	✓	✓	✓	✓
	UART	✓	✓	✓	✓	✓	✓
SD	UHS-I	✓	✓	✓	✓	✓	✓
	UHS-II					✓	✓

●High Speed Interface Macros

Category	Function	Process Technology					
		90nm	65nm	55nm	40nm	28nm	16nm/12nm
USB	USB3.1 Gen2 Host/Device					✓	✓
	USB3.1 Gen1 (USB3.0) Host/Device		✓	✓	✓	✓	✓
	USB2.0 Host/Hub/Device	✓	✓	✓	✓	✓	✓
Ethernet	Gigabit Ethernet MAC	✓	✓	✓	✓	✓	✓
Video	HDMI2.0	✓	✓	✓	✓	✓	✓
	HDMI2.1					✓	✓
	V-By-One HS				✓	✓	
	FPD-Link	✓	✓	✓	✓	✓	
LVDS	LVDS	✓	✓	✓	✓	✓	✓
	SubLVDS	✓	✓	✓	✓	✓	✓
MIPI	DSI TX	✓	✓	✓	✓	✓	✓
	CSI-2 TX/RX	✓	✓	✓	✓	✓	✓
	D-PHY	✓	✓	✓	✓	✓	✓
	C/D-PHY					✓	✓
	M-PHY					✓	✓
PCI Express	PCIe Gen4 RT/EP						✓
	PCIe Gen3 RT/EP					✓	✓
	PCIe Gen2 RT/EP		✓	✓	✓	✓	

Custom SoC

●High Speed Interface Macros

Category	Function	Process Technology					
		90nm	65nm	55nm	40nm	28nm	16nm/12nm
Serial ATA	SATA3 AHCI				✓	✓	✓
	SATA2 AHCI	✓	✓	✓	✓		
	SATA3 Device				✓	✓	✓
DRAM Interface（PHY）	DDR3	✓	✓	✓	✓	✓	✓
	DDR3L	✓	✓	✓	✓	✓	✓
	DDR4					✓	✓
	LPDDR3				✓	✓	✓
	LPDDR4					✓	✓
	LPDDR4X						✓
	HBM2						✓

●Analog Macros

Category	Function	Process Technology					
		90nm	65nm	55nm	40nm	28nm	16nm/12nm
ADC	10bit, up to 600MS/s	✓	✓	✓	✓	✓	✓
	12bit, up to 200MS/s	✓	✓	✓	✓	✓	✓
	16bit	✓				✓	✓
DAC	10bit, up to 220MS/s	✓	✓	✓	✓	✓	
	12bit, up to 110MS/s	✓	✓	✓	✓		
	16bit	✓	✓	✓			
AFE	Audio				✓	✓	
	Video				✓	✓	
	Scanner				✓	✓	
Temperature sensor	+/-5deg.C accuracy (without trimming)		✓	✓	✓	✓	✓
Power management	Vin=3.3V, Vout=1.0-1.2V, Iout≦400mA LDO	✓	✓	✓	✓	✓	✓
	Power on reset				✓	✓	✓
Standard PLL	Fout: ~1200MHz, Fin:10~200MHz	✓	✓	✓	✓	✓	✓
	Fout: ~1600MHz, Fin:16~200MHz	✓	✓	✓	✓	✓	✓
	Fout: ~2400MHz, Fin:16~200MHz				✓	✓	✓
	Fout: ~3200MHz, Fin:16~200MHz					✓	✓
	Fout: ~5000MHz, Fin:20~100MHz					✓	✓
Low Jitter PLL	Fout: ~600MHz, Fin:11~100MHz	✓	✓	✓	✓	✓	✓
	Fout: ~1000MHz, Fin:10~40MHz				✓	✓	✓
	Fout: ~6400MHz, Fin:20~100MHz					✓	✓
Fractional -N PLL	Fout: ~1600MHz, Fin:10~50MHz	✓	✓	✓	✓	✓	✓
	Fout: ~2400MHz, Fin:10~50MHz						
	Fout: ~3200MHz, Fin:10~50MHz					✓	✓
SSCG	Fout: ~1600MHz, Fin:10~50MHz	✓	✓	✓	✓	✓	✓
	Fout: ~2400MHz, Fin:20~50MHz				✓	✓	✓
	Fout: ~3200MHz, Fin:10~50MHz					✓	✓

Interface Macros

DDR Interface

Socionext provides various DDR interface macros from low-to-middle speed forwarding bandwidth to high-speed forwarding bandwidth or low power, with various process technologies. Moreover, we support development for signal quality and cost optimization through design support by Chip-Package-Board co-design.

● DDR interface macros
  · High-speed/high-bandwidth   DDR3/DDR4
  · Low power   LPDDR4X/4/3/2 DDR3L
  · DFI compliant (all macro)
  · Compatible with many different DRAM configurations and PKG options, such as Fly-by, PoP, and DIMM thanks to the PHY function (training function).

● DDR interface design support (Chip-Package-Board codesign)
  · Timing verification : Verifies the timing of all DDR-IF systems including delays between LSI I/O and DRAM
  · Power Integrity : Optimizes the parasitic inductance, resonant frequency, and power supply (PKG, PCB) impedance as part of the power supply impedance design
  · Signal Integrity : Optimizes Driver strength, terminator resistance, and interconnect topology
  · Bus switching verification
                   : Optimizes the write and read bus switch timing

DDR Interface Configuration Diagram
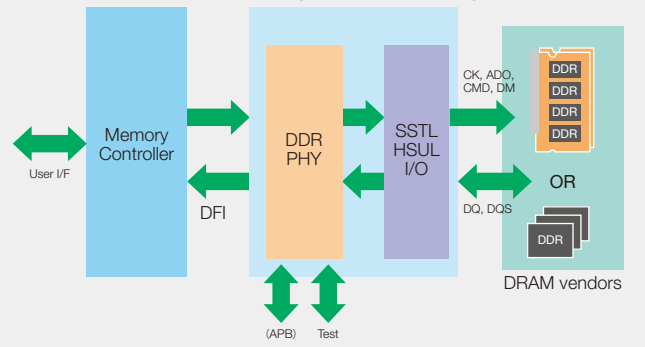
LPDDR4-3733 DQ Waveforms
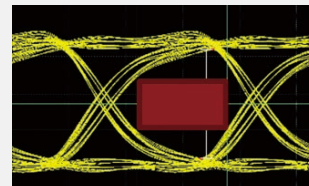
Bus Switching Waveforms
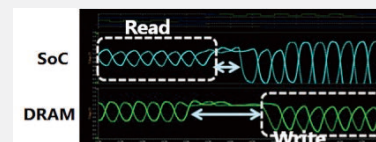
Memory Controllers

Socionext provides various memory solutions for system optimization. We also offer consulting services on memory systems including memory channels and the system bus to maximize SoC performance.

● Memory controller IP
  · Controller for maximizing high DRAM utilization

● QoS-Arbiter IP
  · High performance QoS-Arbiter featuring multiple functions

● BusIP
  · Original low power consumption bus with high layout flexibility

● MonitorIP
  · Visualizes memory system performance in real-time
  · Monitors performance (bandwidth, latency) and provides an environment for tuning parameters

Custom SoC
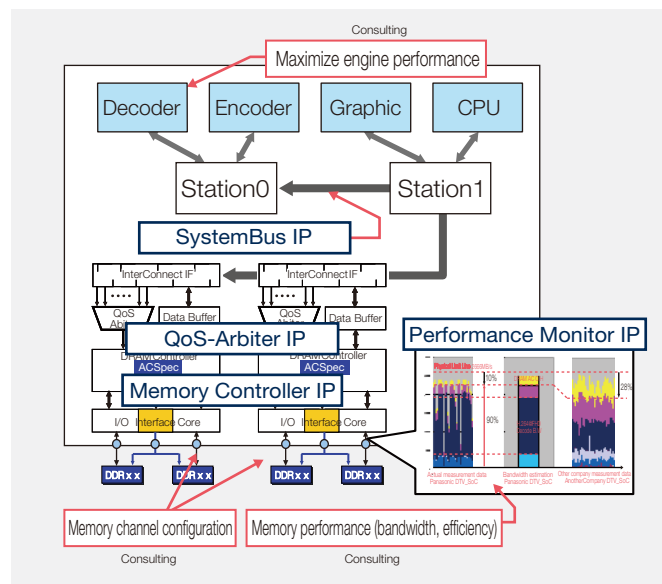
MIPI Interface

This high-speed interface is used to build a camera and display system by combining high-speed, high resolution CMOS image sensors. This interface provides a solution for highly expressive images.

● MIPI D-PHY TX macro

Small footprint, high-performance macro with the maximum speed of 4.5 Gbps

- 4-data lane + 1-clock lane configuration
- Transmission speed: 80 Mbps to 4.5 Gbps per lane
- Equalization function
- The world's smallest footprint
- D-PHY2.0 compliant

PCI Express Interface

As a result of the recent rapid improvement in CPU processing capability and an increase in the need for high capacity data transfer, it has become extremely difficult to achieve the expected system performance with existing buses. The PCI Express technology is a high-speed interface capable of transferring several hundred megabytes of data that can overcome this issue.

Socionext's PCI Express macro supports up to 8 GT/s (Gen3) and passed the PCI Express standard compliance test hosted by the Peripheral Component Interconnect Special Interest Group (PCI-SIG), and its interconnectivity and reliability have been confirmed with many PCI Express interfaces.

● PCI Express LINK macro

- Compliant with the PCI Express Base Specification rev.3.0 standard specification
- Support for x1, x4, and x8 lanes
- DualMode (RootComplex or Endpoint is selectable)
- Possible to select AMBA3 I/F as the user interface
- Built-in DMAC

● PCI Express PHY macro

- Maximum transfer bit rate of 64 GT/s
- High-speed signal transmission with the de-emphasis function is guaranteed
- The LINK macro interface is compliant with the PIPE3 and PIPE4 standard specifications

D-PHY TX Output Waveforms at 4.5 Gbps
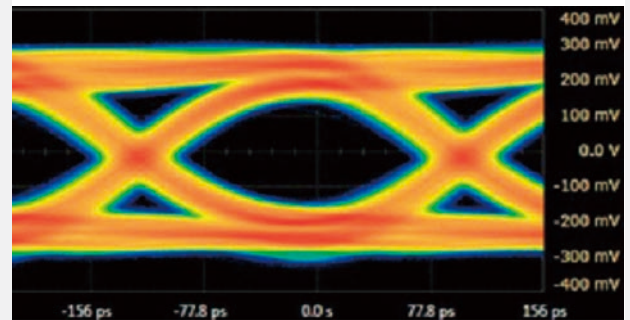
PCI Express Gen3 Evaluation Environment
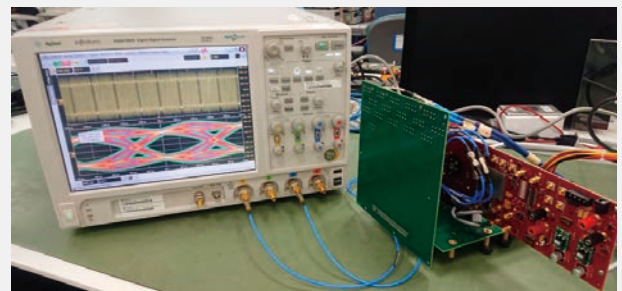
10G-28Gbps SerDes Interface

With transmission performance of 10Gbps–28Gbps per channel and a configuration comprised of multiple channels, we provide a high-performance SerDes macro for constructing 100G/200G/400G optical networks or 100G Ether systems.

The built-in low-jitter, high-performance PLL enables robust transmission up to 28 Gbps per channel.

It also supports various standards including OIF-CEI-11G-SR, OIF-CEI- 28G-SR, OIF-CEI-28G-VSR, IEEE802.3ba CAUI, IEEE802.3bm CAUI4, XFI and so forth.

- ×1, ×4 lane configuration.
- Comprised of Transmitter/Receiver/PLL and capable of bidirectional communication with 1 macro.
- Up to 112.8 Gbps per macro (for unidirectional, ×4 configuration).
- Support for power-down control on each lane.
- Support for power-down control for the entire macro.
- Implementing Clock-Data Recovery for each Receiver lane.
- Transmitter Equalization supported.
- Receiver Equalization supported.
- Built-in termination resistor in Transmitter/Receiver.
- Organic flip chip package.
  (0.8 mm/1.0 mm Ball Pitch, HDBU Package)
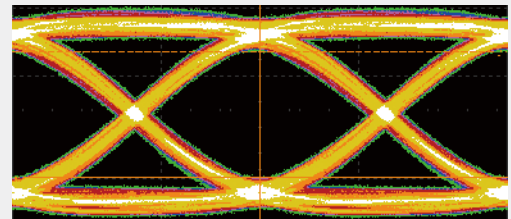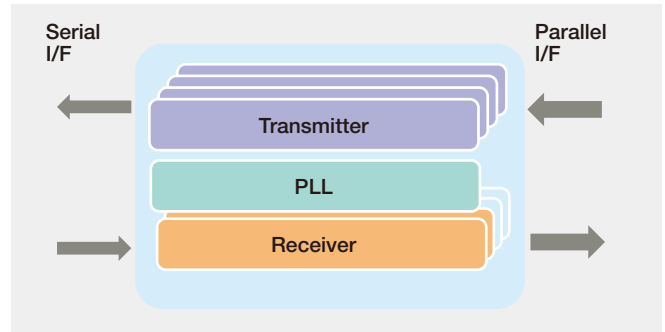
28 Gbps Output Waveforms with Test Chip

Custom SoC

Analog Macros

We offer various analog macros (data converter, power management, temperature sensor, analog front-end) for our customers' development to address various applications including communication, image processing, sensors and control.

- All macros are silicon verified.
- Implemented on many custom SoCs with a track record in mass production.

Data Converters

We offer various data converter macros addressing low power consumption and a small area which are demanded in SoCs.

● **Pipeline & high speed SAR ADC**
- 10-bit/12-bit resolution, maximum 600MSPS conversion rates
- The world's smallest class power consumption

● **ΔΣ ADC**
- Applicable to 16bit to 24bit resolutions
- Power consumption of up to 1 mW with high precision SINAD 85 dB

● **ΔΣ DAC**
- Applicable to 16bit to 24bit resolutions
- SINAD 90 dB. Power consumption is 1 mW or less

Power Management

We offer various power management macros that enable single power supply development which is demanded in SoCs.

● **LDO for low-noise power supply applications**
- Lineup of small-area versions such as the integrated I/O type
- Safety protection functions such as short-circuit detection
- Supports power supply to analog IPs such as ADC and PLL

● **Power-ON reset**
- Customizable voltage-detection level and reset time
- Supports brown-out reset

Data Converters
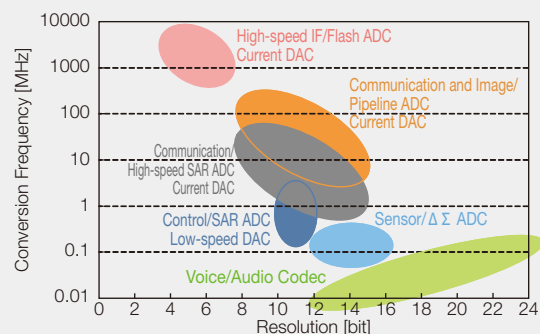
Example Application of Power Management Macro
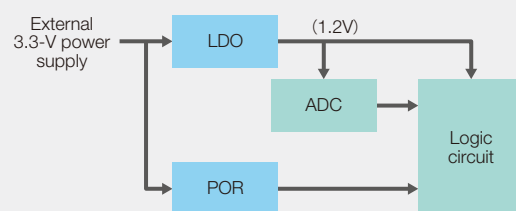
Sensors and Analog Front-End (AFE)

We offer a sensor macro for measuring temperature and voltage inside the chip and a low power-consumption AFE for processing signals from various external sensors.

● Temperature sensor macro
- Can monitor temperature inside the chip at high resolution (0.125° C)
- Low power consumption and small area allow installation of multiple sensors on one chip
- Realizes temperature-dependent voltage and frequency control system

● Scanner AFE
- Supports both CCD and CIS
- Includes gain and offset adjustment function
- Comes with 12-bit, 50 MS/s ADC
- Low power consumption (19 mW)

● Custom AFE that supports various sensor signals and external signals
- AFE for optical sensor, humidity sensor, and gyro sensor
- Video AFE
- Audio AFE
- Digital TV AFE

Example Application of Temperature Sensor
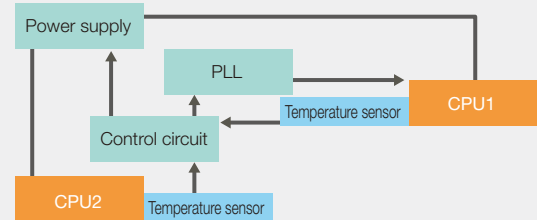
Example Application of Scanner AFE
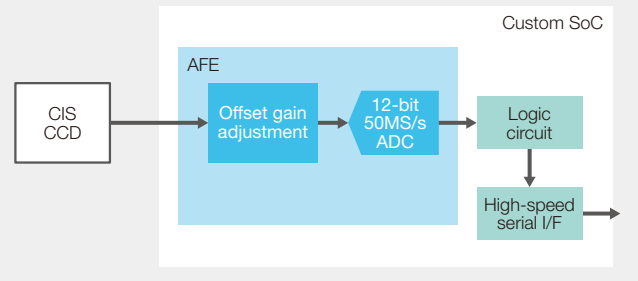
Design Technology

Front-end Design

●Front-end Design kit

We offer a development environment using standard EDA tools as a SoC development environment for customers and a tool we created for improving design efficiency as a design kit. The front-end design kit, which is uniquely optimized by Socionext, enables the development of high performance, small chip size, low power LSIs.

EDA tools supported by Socionext front-end design kit

High level synthesis		Catapult*3, C-to-Silicon Compiler*1, Stratus*1
RTL style check		SpyGlass*2
Functional verification	Verilog-HDL	Incisive Enterprise Simulator*1, Questa*3, VCS-MX,VCS*2
	VHDL	Incisive Enterprise Simulator*1, Questa*3, VCS-MX*2
	CPF/UPF	Incisive Enterprise Simulator-XL*1, Questa*3, VCS-NLP*2
Logic synthesis		Design Compiler*2, Encounter RTL Compiler*1, Genus Synthesis Solution*1
Equivalence verification		Encounter Conformal Equivalence Checker*1, Formality*2
Timing constraint verification		Encounter Conformal Constraint Designer*1, SpyGlass Constraints*2
MV verification		Encounter Conformal Lowpower*1, VC Static Low Power*2
Analysis/debugger		Verdi*2
Netlist check*		SpyGlass*2
Pre-DFT check*		SpyGlass DFT*2

*1: Cadence, Inc.
*2: Synopsys, Inc.
*3: Mentor Graphics Co.
* : We provide a checker we developed in-house to suit the technology.

●Design specification I/F

Designing an SoC requires not only RTL and netlist as logic design data, but the power intent, such as the SDC describing timing specifications including clock frequency, and CPF/UPF containing power supply specifications, including power gating design and multi-power/multi-voltage design. We provide interface files in our unique format for such SDC and power intent. Using such files allows you to improve efficiency in writing and reviewing specifications and quickly verify the consistency between the handed-off RTL, power supply specifications, and timing specifications as well as layout compatibility.

POSS (Socionext format): Improves efficiency in writing and reviewing power supply specifications
Design DS (Socionext's format): Improves efficiency in writing and reviewing timing specifications
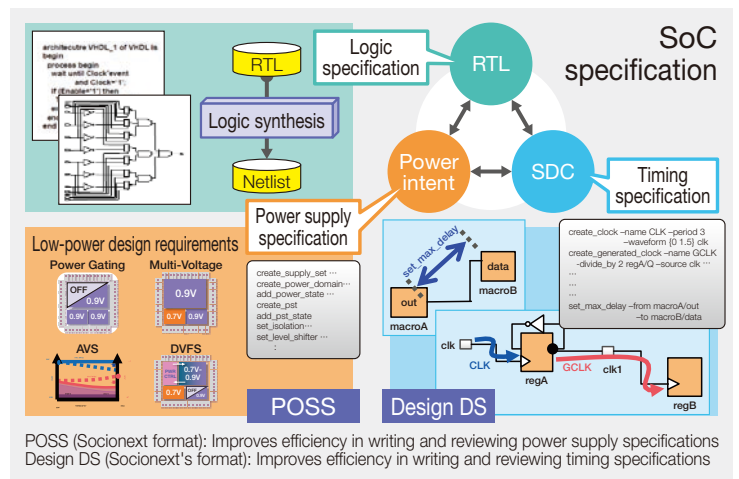
●Physical aware logic synthesis

Due to progress in technology, logic design that takes layout into account is becoming important for improving SoC design efficiency as well as optimizing area and timing. For this reason, we adopt physical aware synthesis that performs optimization by taking the actual layout into account. Through this co-design between the logic design and layout design, we can efficiently design sophisticated SoCs for your product.


Optimistic optimization   Appropriate optimization
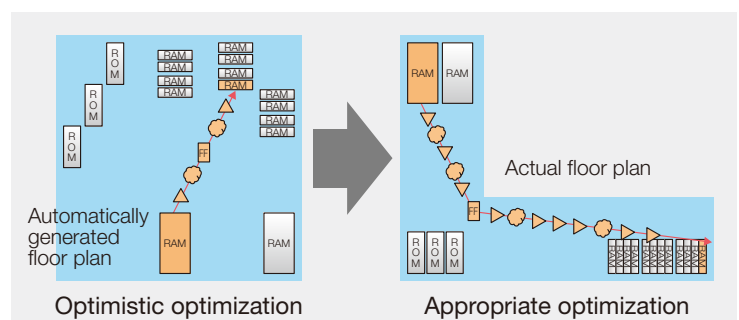
Low Power Design Solutions

The demand for reducing the power consumption of LSIs has been getting stronger in recent years. In our SoC design efforts, we are undertaking various initiatives to meet customers' demands for lower power consumption. In order to achieve low power consumption LSIs, it is effective to combine various kinds of technologies as well as using individual technologies. Socionext's design environment "Reference Design Flow" supports various low power consumption technologies and enables the power consumption of LSIs to be reduced during both operation and standby. By controlling the power supply in particular, we develop methodologies for systematically achieving low power consumption. Also, by fully adopting UPF/CPF, we make low power consumption design, easy for customers while minimizing changes to their design assets. The use of UPF/CPF allows for high reliability designs even with low power consumption technology, which it has been extremely difficult to verify in the past.

●Multi voltage design

With this technology, different voltages are supplied to an LSI to reduce power consumption during the operation of circuit blocks for a high-speed operation circuit block, a high voltage is supplied, and for a low-speed operation
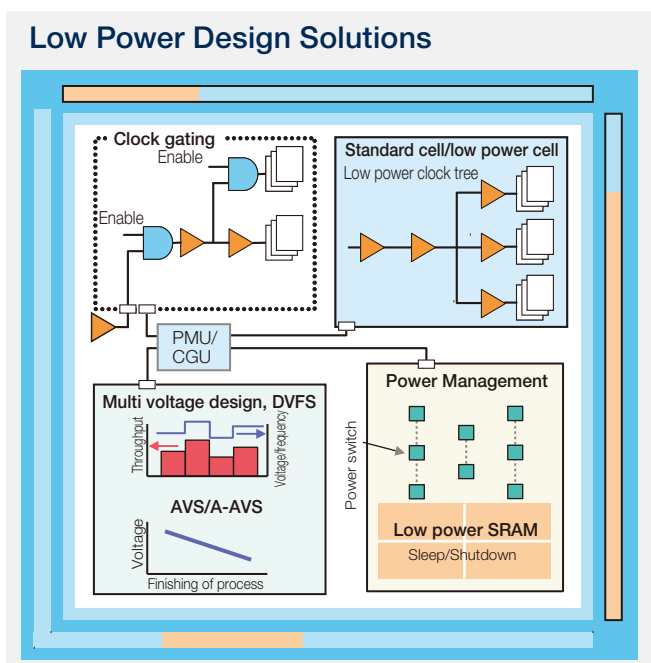
Low Power Design Solutions

Design Level	Design Technology		
System level design	Memory access reduction Computation reduction Architecture selection Effective use of cache	Power Management	Dynamic Voltage and Frequency Scaling
RTL design	RTL optimization		
Logic synthesis	Netlist optimization Multi power-supply design Clock gating		
Layout	DVFS, AVS/A-AVS Low power standard cell Low power SRAM		

circuit block, a low voltage is supplied.

Using UPF/CPF allows physical design and verification of circuit blocks with different voltages to be performed together, minimizing extension of the development period for low power consumption design.

●Clock gating

Clock gating enables the power consumption of LSIs during operation to be reduced by stopping the supply of clock signals to circuit blocks that do not need to operate.

●Power management

We provide power management technology to control power gating, SRAM sleep, and shut-down mode in a comprehensive manner. By thoroughly eliminating useless, this technology contributes to low power consumption. With its unique power switch controlling system, Socionext's power management technology suppresses the rush current noise generated when the power supply is turned on and off to prevent LSIs from malfunctioning.

In addition, using UPF/CPF allows physical design and verification of circuit blocks that have a power shutdown circuit to be performed together, minimizing extension of the development period.

●Adaptive power supply control (DVFS[*1], AVS[*2]/Advanced-AVS)

We can use DVFS, which is for varying the voltage and frequency according to the required throughput.

Low Power Design Solutions

This technology also adaptively determines the operating voltage according to voltage variation due to manufacturing variability and operates the LSI at the lowest voltage at which its operation is guaranteed, leading to reduced power consumption of the LSI during both operation and standby.

[*1] : DVFS (Dynamic Voltage Frequency Scaling)
[*2] : AVS (Adaptive Voltage Scaling)

●Standard cell

In the area of advanced technology, in addition to the standard cell area, routability contributes to the low power consumption of LSIs.We provide our original standard cell that is far superior to that of other companies. In addition, we offer a rich line-up of cells that are effective for achieving low power consumption of the clock system.

●Low power SRAM

An LSI with high-capacity SRAM may have a problem with the power consumption of the SRAM macro. In such cases, power consumption may be reduced by using a multi-mode SRAM. Multi-mode SRAM features a standby mode, sleep mode, and shut-down mode, as well as a normal operation mode. The standby mode allows for the operating power of an SRAM macro to be 0 by stopping the clock operation inside the macro. In sleep mode, leakage power is reduced by deactivating peripheral circuits of the SRAM macro. Power can only be shut down with an SRAM in shutdown mode. The optimization of the SRAM configuration to be used contributes to low power consumption as well. We help customers select the best SRAM from the logic design phase.

Operating Mode	Function	Effect
Normal	To operate RAM normally	—
Standby	To stop the SRAM operation	The operating power is 0
Sleep	To retain data	Leakage power is reduced to one-third[*]
Shutdown	To shut down the power with only the SRAM	Leakage power is reduced to one-sixth[*]

[*] : Depends on the SRAM structure

●Low power design environment that fully adopts UPF/CPF

Socionext offers a total solution that supports power gating, multi power supply, and multi-voltage design through consistent power supply specification management with UPF[*1] and CPF[*2], RTL simulation for complicated power supply design due to an increased number of integrated IPs, multi power supply verification, and physical design. This solution allows power shutdown verification to be performed based on RTL simulation by managing power supply specifications as separate logical and physical specifications and defining only the logical specification. Verified RTL and the logical specification for the power supply are handed off to physical design, the power supply physical specification that defines the power supply connection is prepared, and then physical design is performed based on these power supply specifications(UPF/CPF). Managing the power supply specification with UPF/CPF in this way and using it through a design flow clarifies the power supply specification and allows for high reliability design.

[*1] : UPF (Unified Power Format) is a standard specification that defines the Low power design guidelines standardized as IEEE Std. 1801. (http://www.ieee.org/)
[*2] : CPF (Common Power Format) is a standard specification that defines the Low power design guidelines standardized as Si2. (http://www.si2.org/?page=811)
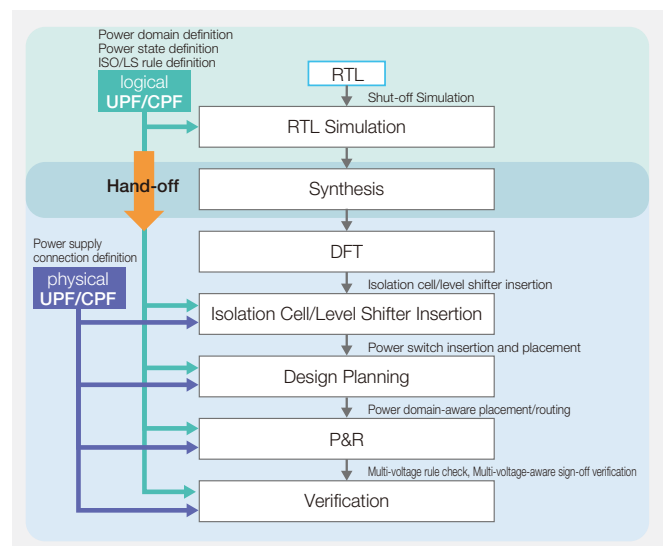
DFT (Design For Test) Technology

SoC testing is becoming more complicated as processes become more refined, circuit scale increases, circuit operation becomes faster, and much less power is consumed. To resolve this issue, in addition to compressed scan, memory BIST, and boundary scan DFT, we perform high quality testing using various types of DFT technology for improved test quality and yield.

[DFT Technologies Adopted by Socionext]

● At-speed and low power test technologies for improved test quality
　・Test using on-chip PLL clocks
　・Test that controls power consumption during testing
● Memory redundancy repair process and fault diagnosis technologies for improved yield

Boundary scan | IO
Memory BIST
Memory
OCC | Compressed scan
PLL | Logic

Yield improvement technology:
Memory redundancy relieving process can be performed.

Low power test technology:
Test that controls power consumption during testing is supported.

At-speed test technology:
Test using on-chip PLL clocks is supported.
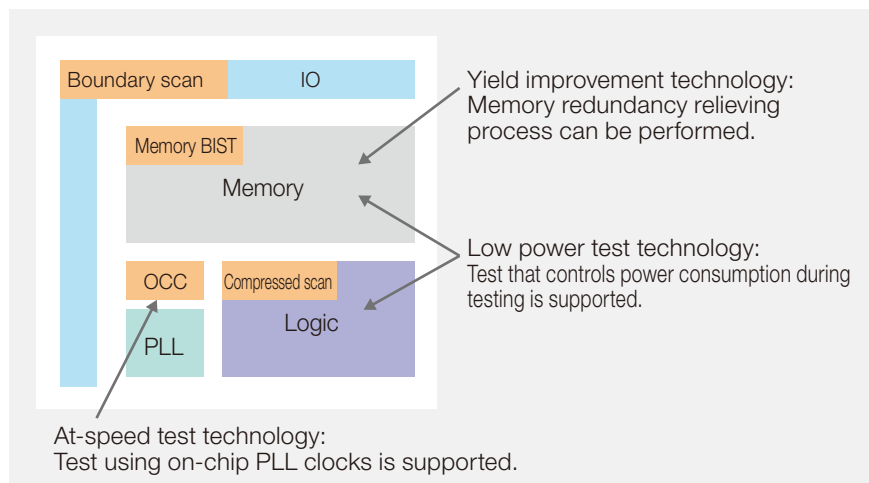
Back-end Design

We layout customer design with our high-accuracy analysis technology, high performance synthesis, placement, routing, and high speed technology, and low noise design technology.

●Physical aware logic synthesis

Due to the increase in circuit size and routing load caused by the progress of refinement, the gap between the estimate at the time of logic synthesis and layout is widening. At Socionext, we minimize the gap with the layout by taking into account layout information from the logic synthesis step. This allows for early confirmation of timing convergence, thereby shortening the development period.

●UPF and CPF support

We support UPF and CPF and perform physical design and physical verification based on power supply specifications for which functional verification is conducted. This enables high design quality to be achieved even for complex low power consumption technologies.

●Multiple mode/corner-aware optimization

As refinement progresses, the processes, voltage, and temperature conditions (corner conditions) that should be taken into account are increasing. In addition, the number of operation modes is increasing to enhance multifunctionality and secure the reliability of LSIs. In our physical design, placement, routing, and optimization that take into account multiple corner conditions and operation modes are performed. This makes it possible to reduce the iteration of timing optimization due to conflicts between different corners and modes, which shortens the development period.

●Power rail analysis/crosstalk noise analysis

As refinement progresses and voltages become lower, the delay variation due to an IR drop (voltage drop) in LSIs and crosstalk noise increases.
Through high accuracy IR drop and crosstalk noise analysis, we have verified that they do not affect system operations.

Physical aware logic synthesis

Conventional logic synthesis
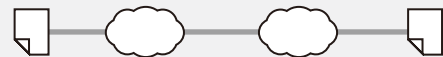
Physical aware logic synthesis
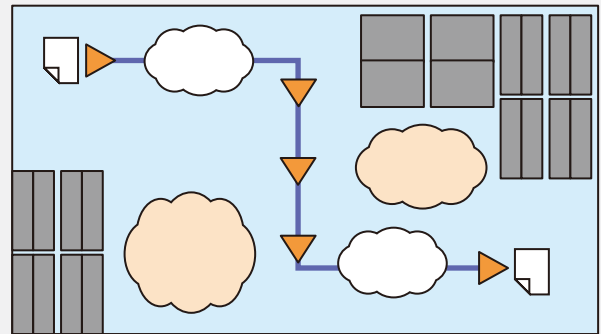
Multiple Mode/Corner Optimization

Corner conditions

Timing constraints

Power rail analysis/Crosstalk Noise Analysis

Design Technology
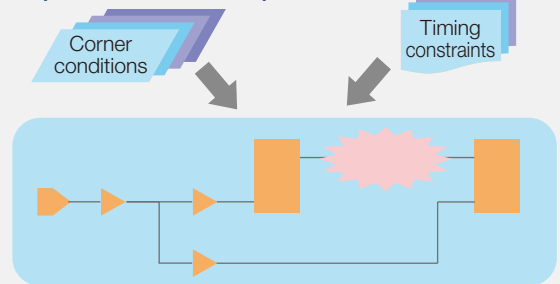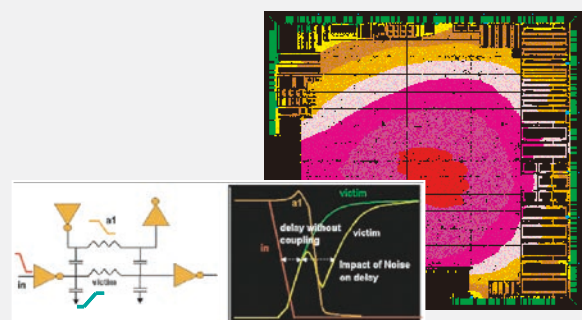
# Chips designed with noise in mind, packages, and PCB co-design

Socionext achieves perfect operation on the first attempt through LSI development based on the chip, package, and PCB codesign flow. While offering a good forecast for design through reference design, we develop and improve LSI models (IBIS, timing model, LSI power supply model) necessary for transmission line analysis of DDR4 and other memory interfaces and USB3.0 and other SerDes interfaces to achieve total optimization in each phase of design based on integrated chips, packages, and PCB analysis. This allows for an issue that used to only be discovered in the actual design phase to be addressed in the prototyping phase.
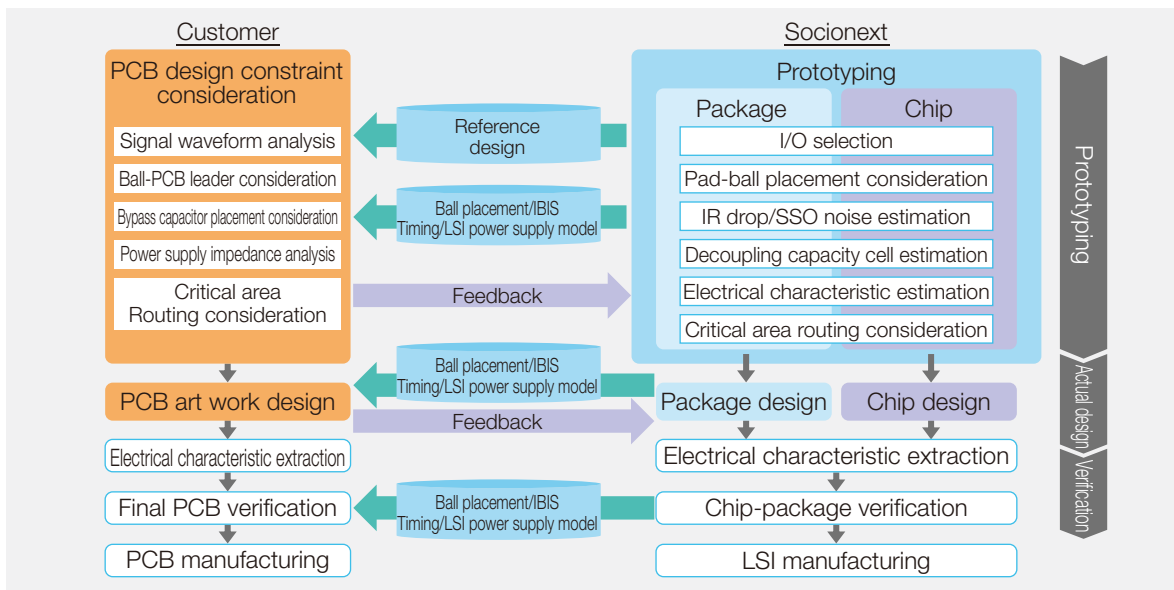
We offer customers IBIS and a timing model early on in the design stage so that they can conduct transmission line analysis taking timing into account.

DDR4 Waveform/Timing Analysis by Customer

USB3.0 Waveform Analysis by Customer

IBIS-AMI
Channel Analysis
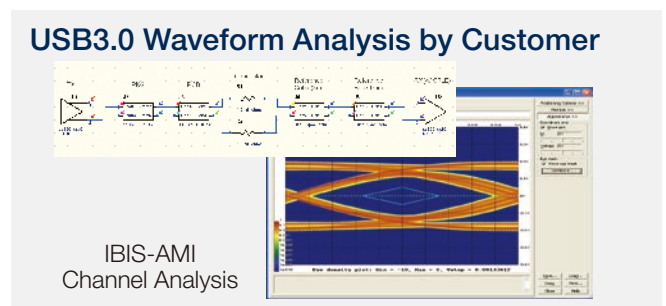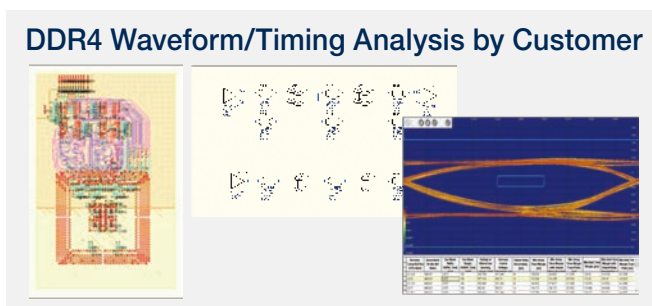
The use of IBIS5.0 and an LSI power supply model (chip and package) for PCB power supply impedance analysis and SSO noise analysis allows customers to perform high accuracy development in a short TAT.

PCB Power Supply Impedance Analysis (SPICE Netlist vs. IBIS5.0)

SSO Noise Analysis (SPICE Netlist vs. IBIS5.0)
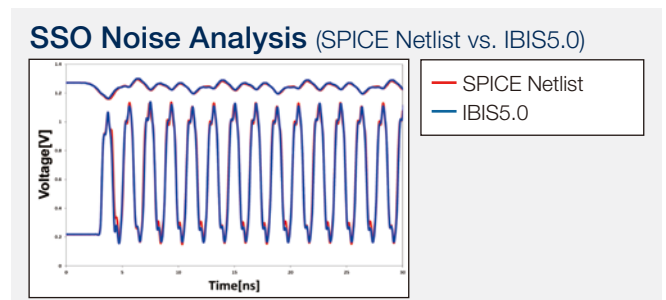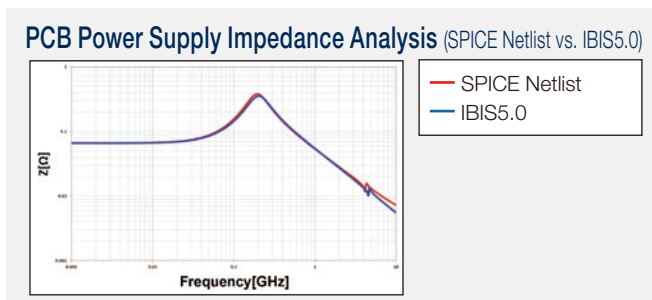
Simulation

Utilizing advanced simulation technologies, we offer the best package solution.

●Mechanism simulation

Incorporating mechanism simulation into package design allows customers to propose high reliability packages.

Case) Stress Analysis of Solder Joint Sections

Model

Heat sink

PKG board

Paste

LSI

Solder bump

Underfill

Analysis results
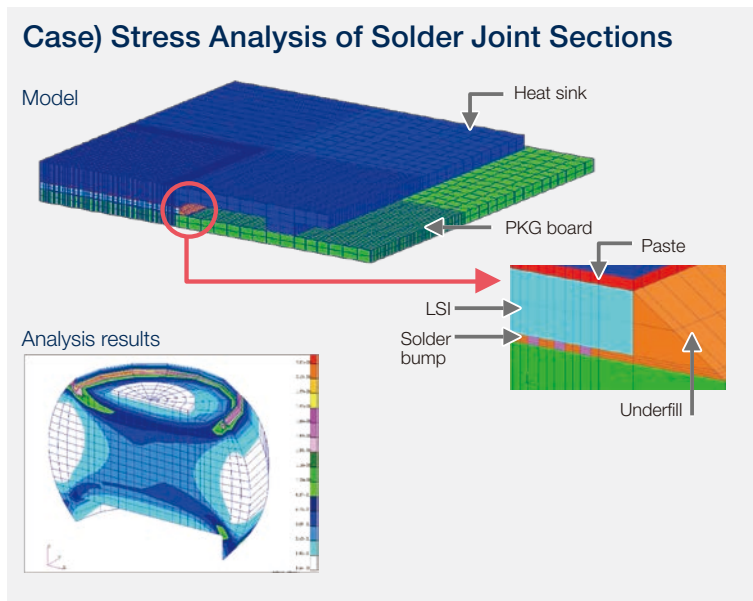
●Thermal design simulation

By combining actual measurement of thermal resistors and thermofluid simulation, we perform high accuracy thermal resistance analysis reproducing the operating environment of products.

JEDEC Environment

Model

Case   inside   except HS

Profile

with FIN+FAN

with Heatsink TV Case

Thermal Distribution on Chip
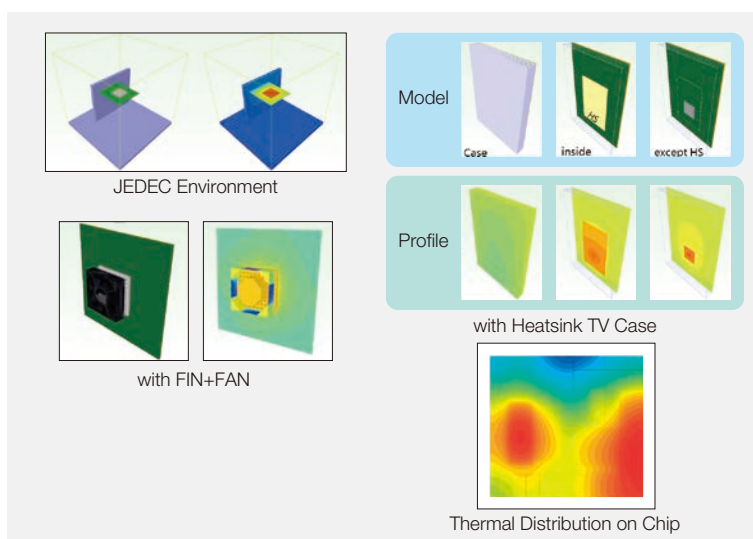
●Thermal resistance measurements

Measurement of transient thermal resistance values in accordance with the JEDEC standard JESD51-14 is possible.

Manufacturing Technology Package

Advanced Processes

Technologies and Device Products

Our device products from 90 nm to 12 nm include standard cell types supporting a wide range of technologies. Socionext is working with multiple foundry partners. Thanks to the synergy effect of their manufacturing capability and the quality control system and design engineering ability of Socionext, we will continue to lead the LSI industry in design and manufacture of cutting-edge custom SoCs.

●Standard cell

Technology	Device Product Name	Power Supply Voltage (Typ.)
7 nm FinFET CMOS	T.B.D.	T.B.D
12 nm FinFET CMOS	CS661 series	+0.7V±0.07V / +0.8V±0.08V
16 nm FinFET CMOS	CS602 series	+0.7V±0.07V / +0.8V±0.08V
28 nm Metal Gate CMOS	CS407 series	+0.8V±0.08V / +0.9V±0.09V
28 nm Metal Gate CMOS	CS405 series	+0.9V±0.09V
40 nm Si Gate CMOS	CS302 series	+1.1V±0.1V
55 nm Si Gate CMOS	CS251 series	+1.2V±0.1V
65 nm Si Gate CMOS	CS201 series	+0.9 V to +1.3 V (supports a wide range)
90 nm Si Gate CMOS	CS101 series	+0.9 V to +1.3 V (supports a wide range)

●Gate scale comparison

Number of gates installed
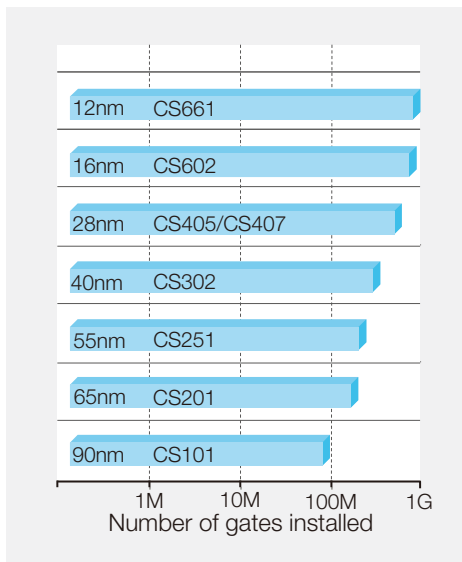
●Power consumption comparison
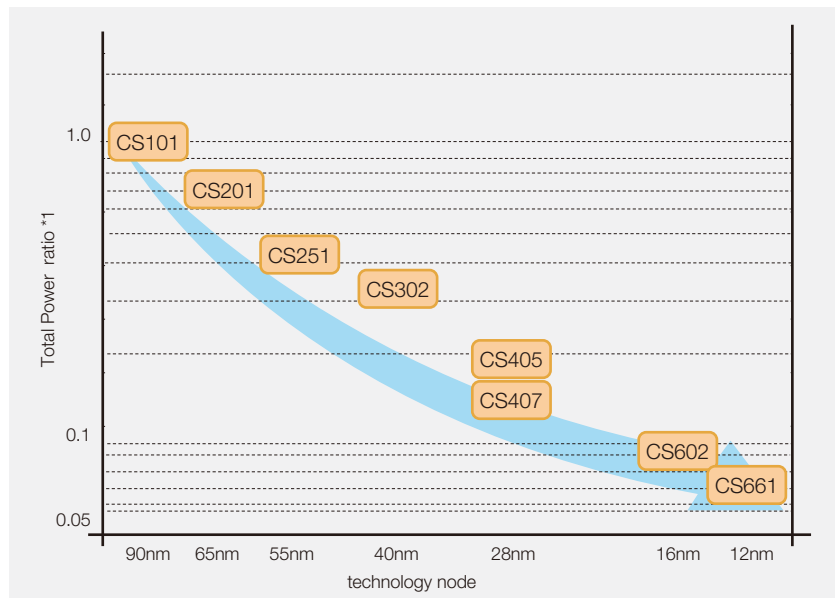
*1 : The vertical axis shows the relative ratio of each technology using the total power (sum of the dynamic component and leakage component) of CS101 as the criterion

Advanced Packages

Package System

From high performance models for high end use to high cost performance models for consumer use, we provide a wide range of packages.

Package Type	Package Structure	Thermal Resistor θja[*1] (°C /W)	Example Purposes
FC-CBGA		7〜	Servers, high-speed large capacity network, etc.
FC-PBGA (Low loss tan δ BU)		7〜	Servers, high-speed large capacity network, etc.
FC-PBGA (Conventional)		9〜	Factory automation, office equipment, medical care, health care, satellite broadcasting, digital TVs, set-top boxes, digital signage, etc.
TEBGA		13〜	Factory automation, office equipment, medical care, health care, satellite broadcasting, digital TVs, set-top boxes, digital signage, etc.
PBGA		15〜	Factory automation, office equipment, medical care, health care, satellite broadcasting, digital TVs, set-top boxes, digital signage, etc.
FBGA		17〜60	Mobile devices, digital still cameras, camcorders, action cameras, drones, security devices, wearable devices, etc.
FCCSP		17〜60	Mobile devices, digital still cameras, camcorders, action cameras, drones, security devices, wearable devices, etc.
QFN		20〜40	Mobile devices, digital still cameras, camcorders, action cameras, drones, security devices, wearable devices, etc.
WL-CSP		25〜60	Mobile devices, digital still cameras, camcorders, action cameras, drones, security devices, wearable devices, etc.
LQFP TEQFP		15〜100	Mobile devices, digital still cameras, camcorders, action cameras, drones, security devices, wearable devices, etc.

High end → Consumer use

[*1]: Reference value. The thermal resistance value varies depending on the chip size or package specification. Inquire to us regarding individual cases.

Package Roadmap

Through a strong partnership with outsource assembly and test (OSAT) in Japan and overseas, we provide packages with well balanced technology, cost, quality, and reliability.

Extract functions required for applications

Server/Network

TV/MFP

Mobile/IoT

Automotive

Current solution	Next generation

FCBGA

P・TEBGA

FBGA・FCCSP

WL-CSP

LQFP/QFN
FCBGA
P・TEBGA
FBGA
SiP / Module

Memory mount / High density → POP

Embedded passive → Module

SiP

Wide bus memory / Embedded die → POP comprising intermediate board

Wide bandwidth → Si-photonics

Wide-band wide-bus memory → 2.xD/3D

Wide bus memory / Thin design → FO-POP

High density (pseudo-SoC) → FOWLP

Electrical characteristic → FOWLP

＊POP : Package On Package

＊FOWLP : Fan Out Wafer Level Package

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